

LYON-External

CPU : Intel PENRYN

Chip Set : Intel CANTIGA PM + ICH9M

Remarks : Montevina Platform (NB9M)

Model Name : LYON-Ext

PBA Name : MAIN

PCB Code : TPT : BA41-00919A

GCE : BA41-00920A

NAN : BA41-00921A

Dev. Step : MP

Revision : 1.0

T.R. Date : 2008.06.09

DRAW	CHECK	APPROVAL

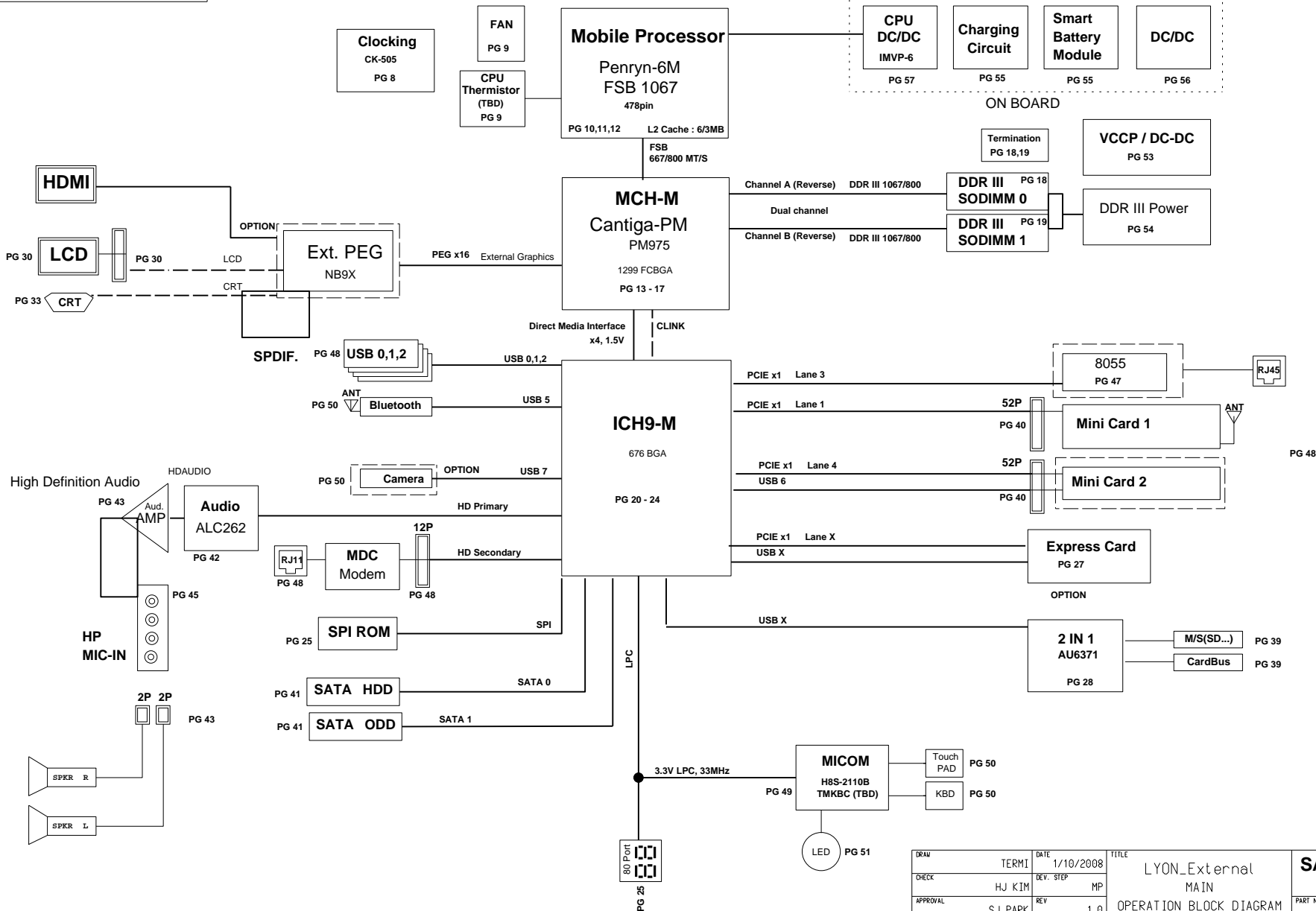
■ Owner : SEC Mobile R & D

Signature : X

DRAW	TERMI	DATE	1/10/2008	TITLE LYON_External COVER	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
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DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	MAIN	ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0	OPERATION BLOCK DIAGRAM	PART NO.	BA41-00920A
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices			
Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails	
VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
	SYSTEM PORT 0	0	NC
	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
	SYSTEM PORT 2	2	NC
	NC	3	LOM
	NC	4	Mini Card 2 (ROBSON or DVB-T)
	Bluetooth	5	NC
	Mini PCI Express 2		
	Camera		
	NC		
	NC		

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I C / SMB Address			
Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

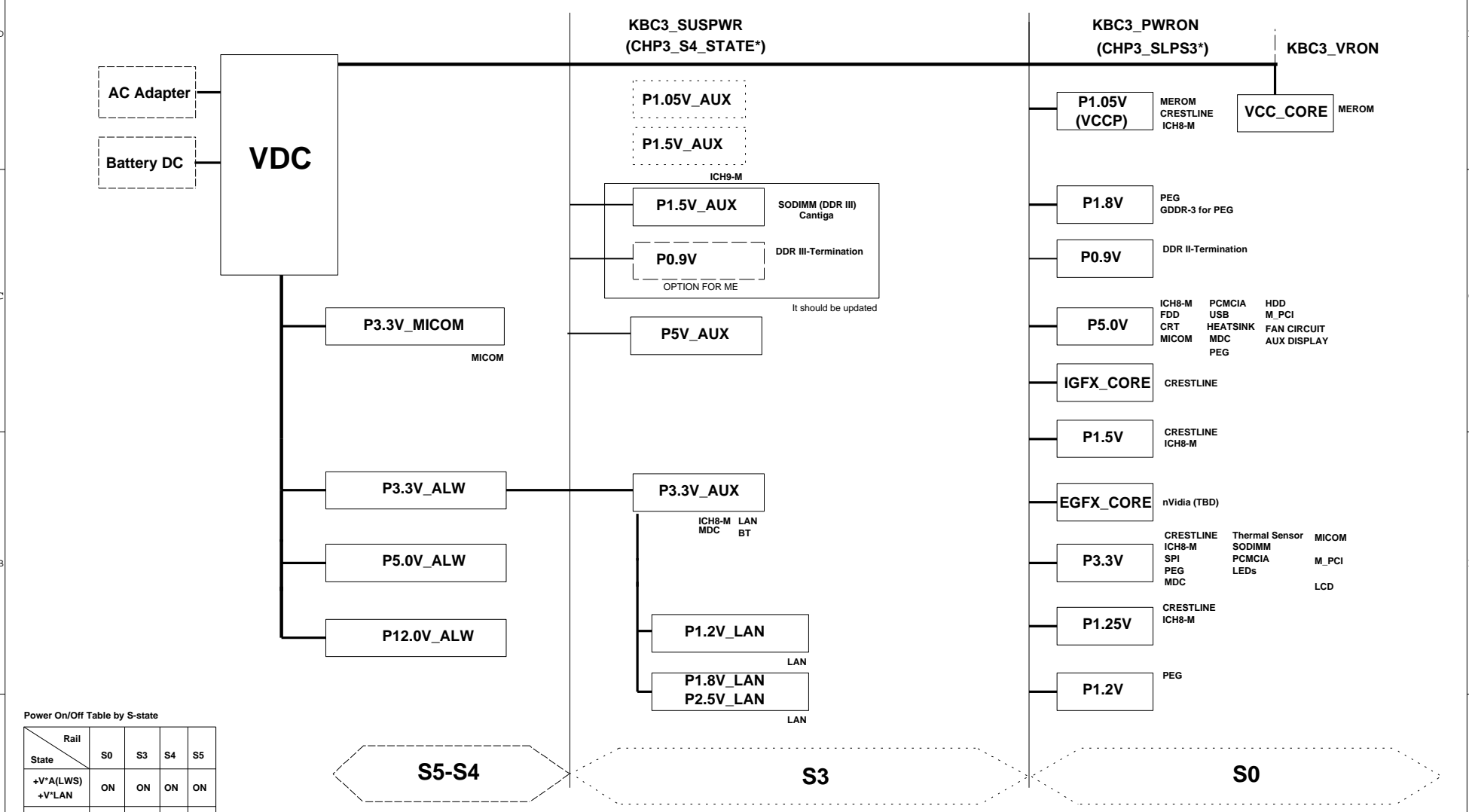
REVISION HISTORY

See rev notes for more information.

DESIGN	TERMI	DATE	1/10/2008	TITLE	LYON-External CHIPSET POWER UNDEFINED	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

Rail	S0	S3	S4	S5
State				
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

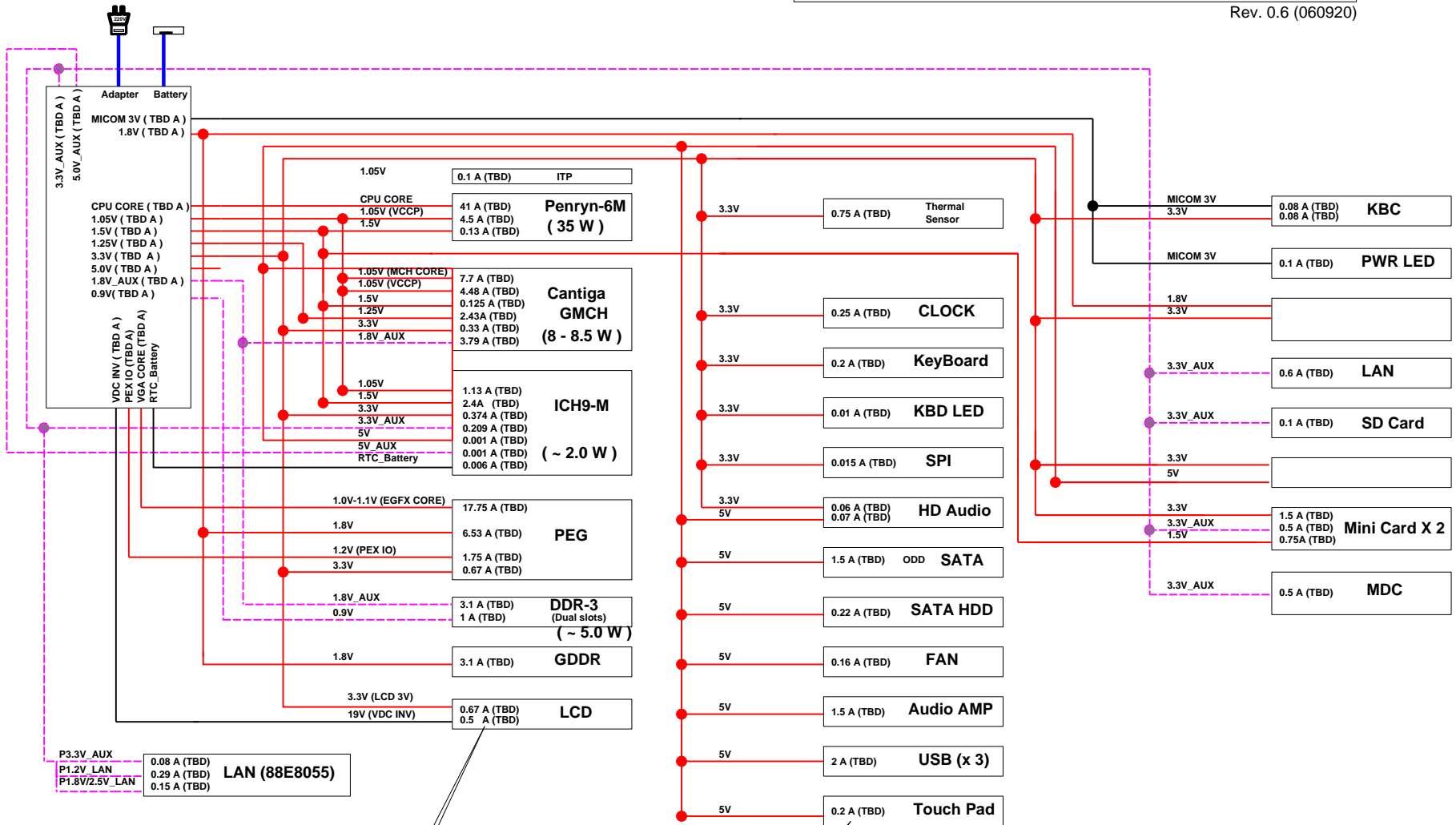
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TERMI		1/10/2008	LYON_External		
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APPROVAL	SJ PARK	REV	1.0	POWER DIAGRAM	
MODULE CODE		LAST EDIT			PART NO. BA41-00920A
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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

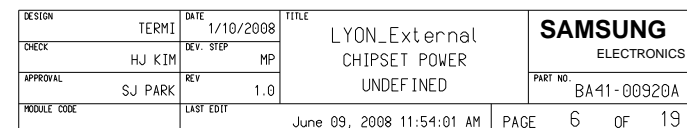


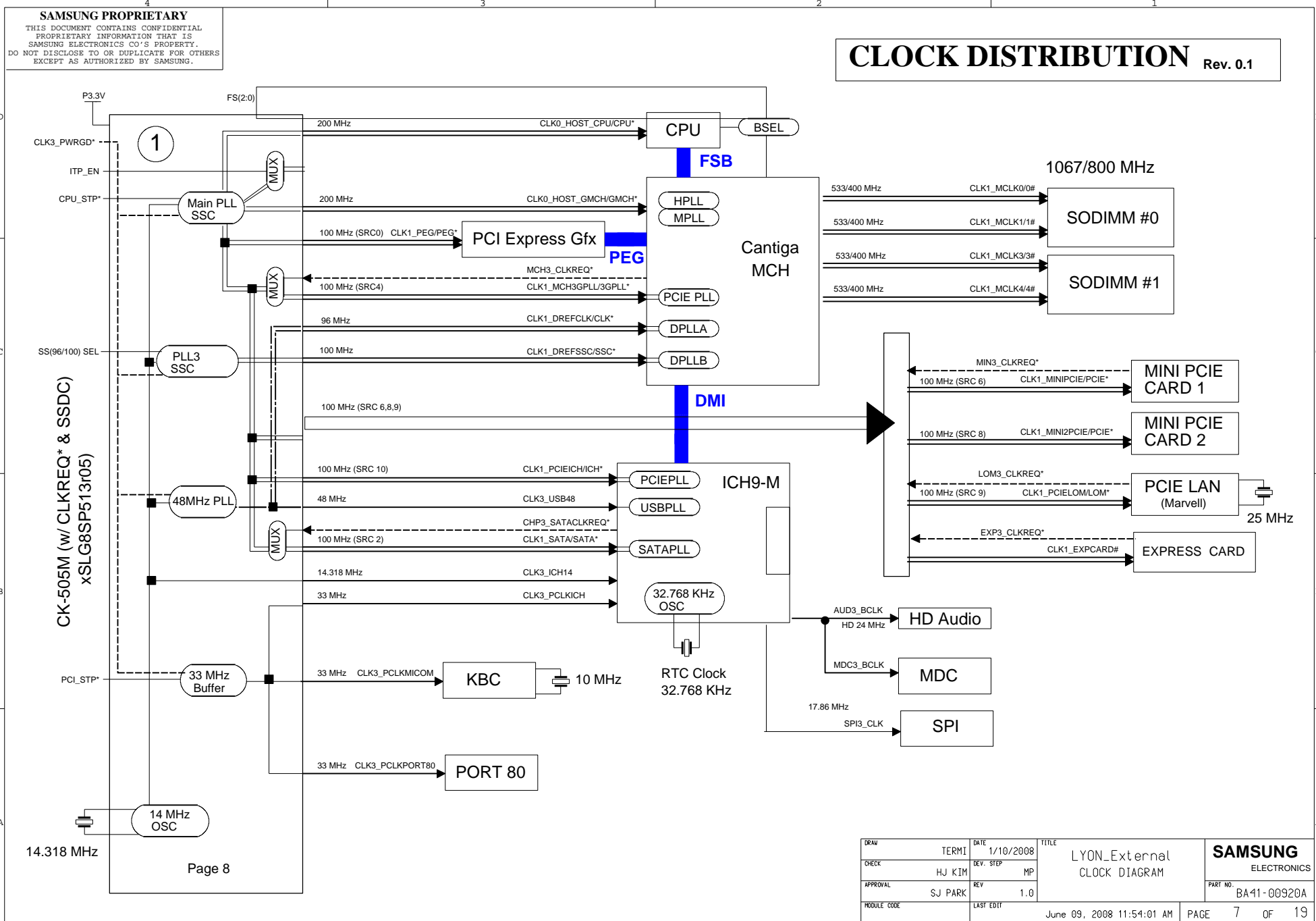
Value by Datasheet/Application notes (Value by measurement)

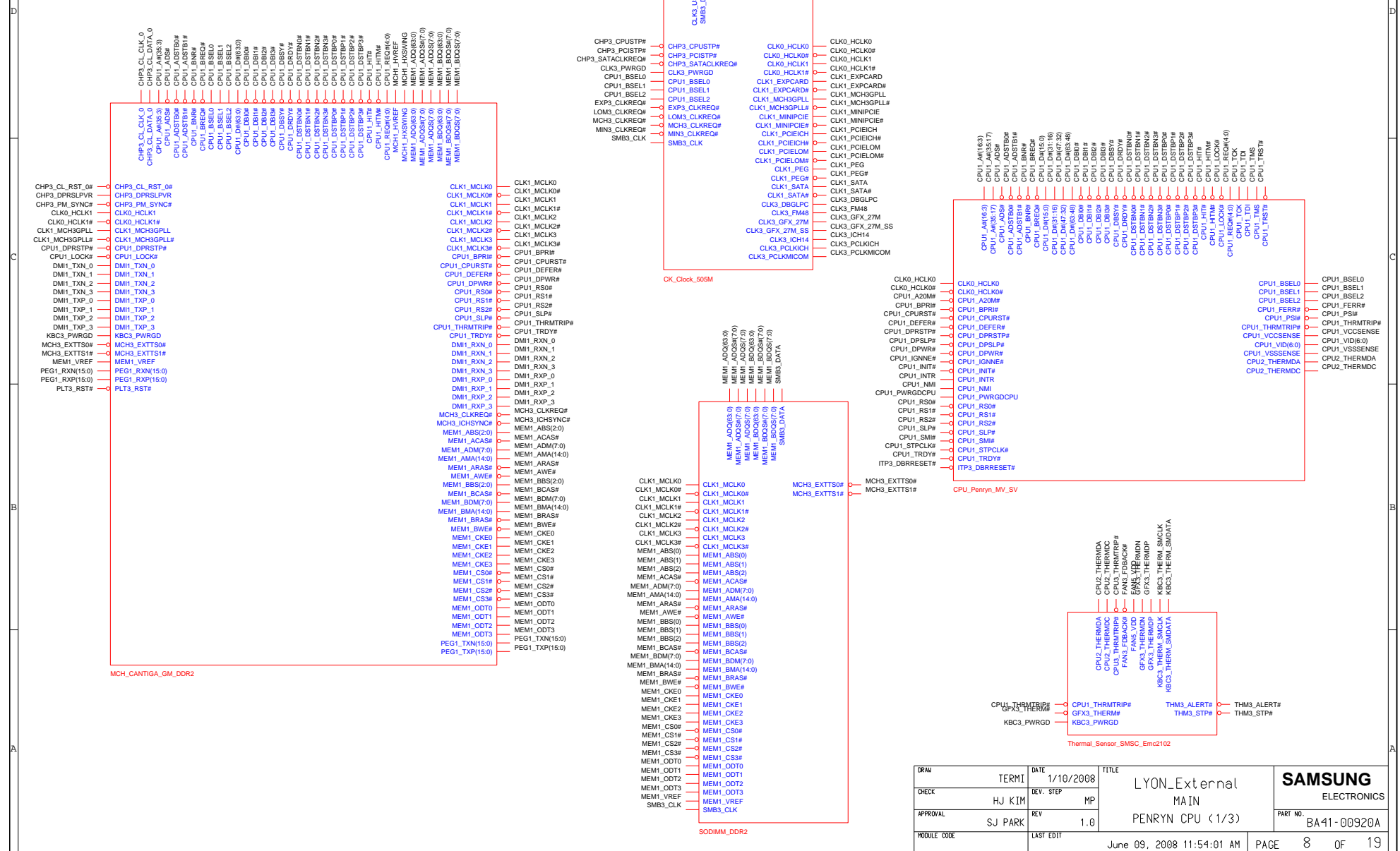
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APPROVAL	SJ PARK	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM			BA41-00920A
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Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*





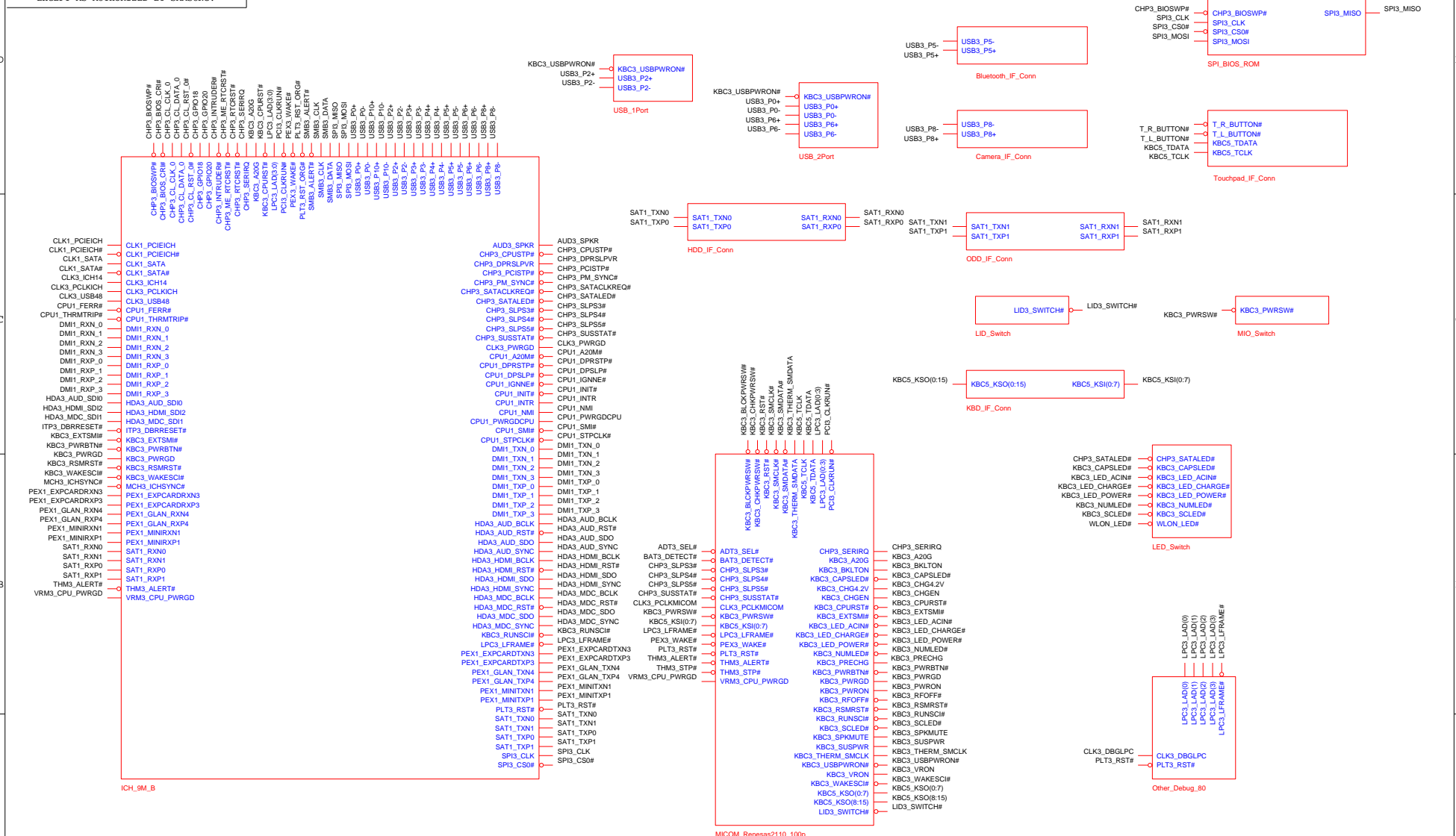



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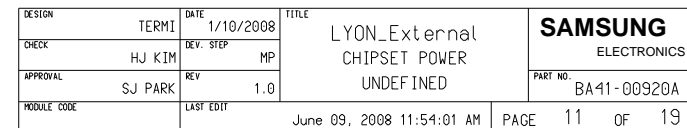
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APPROVAL	SJ PARK	REV	1.0				PART NO.	BA41-00920A
MODULE CODE	LAST EDIT		June 09, 2008 11:54:01 AM				PAGE	9 OF 19

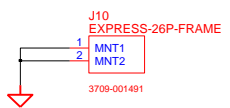
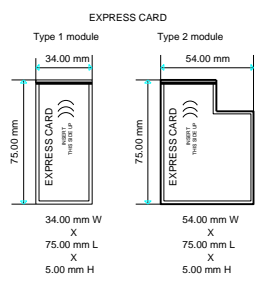
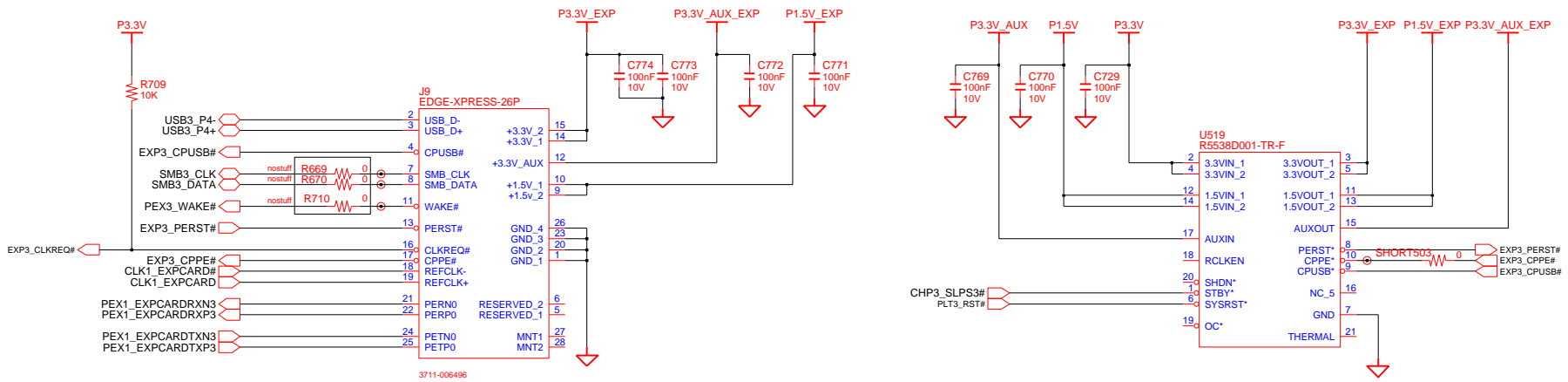
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Graphics Memory Nvidia

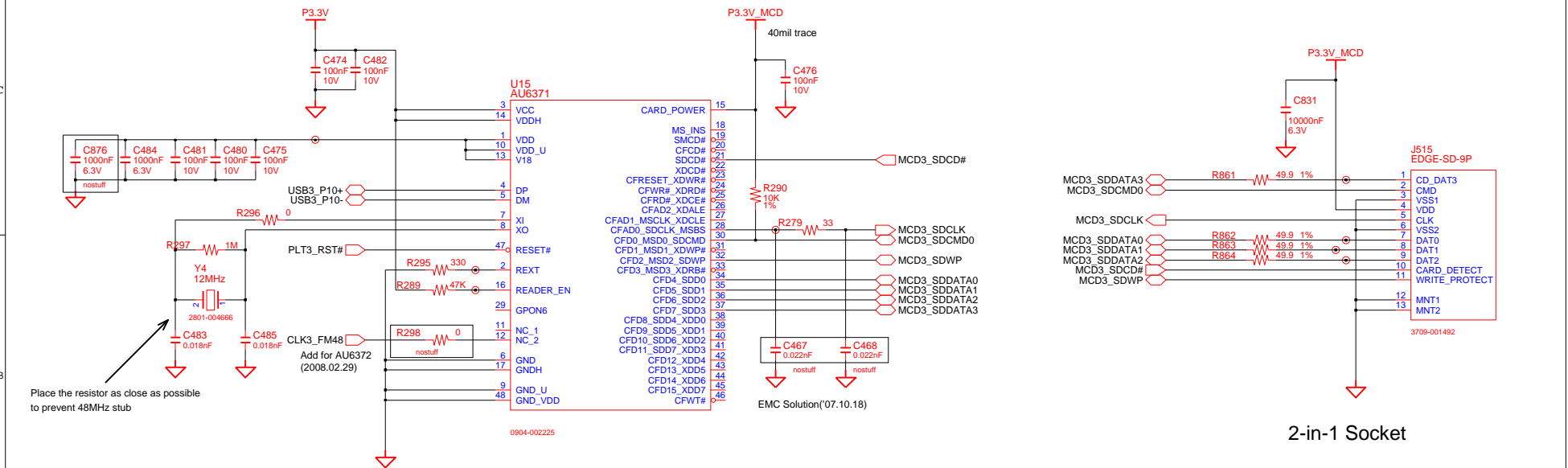
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CHECK	HJ KIM	DEV. STEP			MP
APPROVAL	SJ PARK	REV			1.0
MODULE CODE	LAST EDIT				June 09, 2008 11:54:01 AM



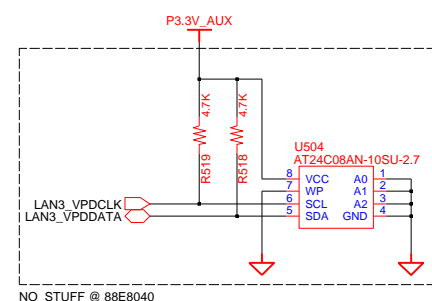
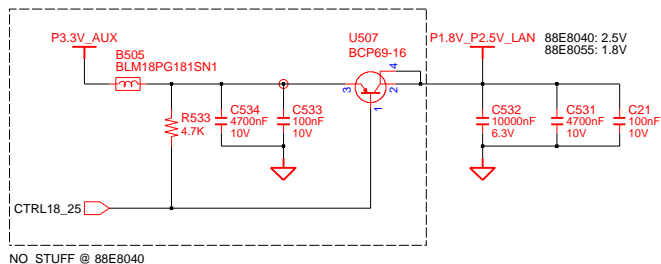


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MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	12 OF 19	

2 IN 1 CARD

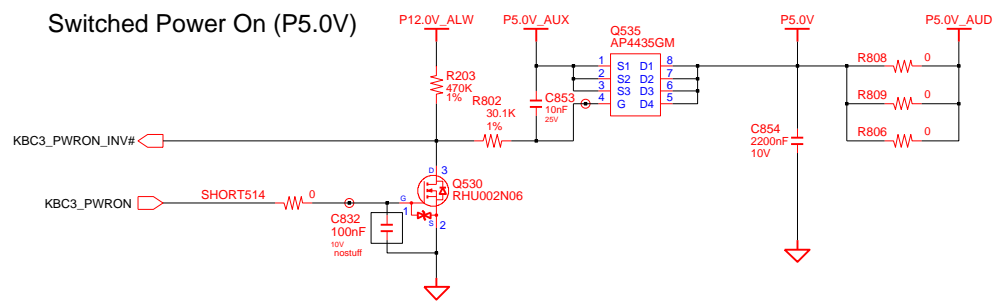


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APPROVAL	SJ PARK	REV	1.0		2 in 1 Socket	PART NO. BA41-00920A
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	13	OF 19

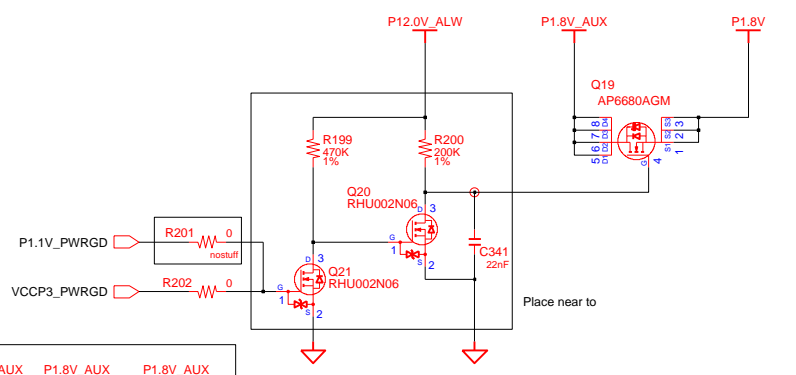
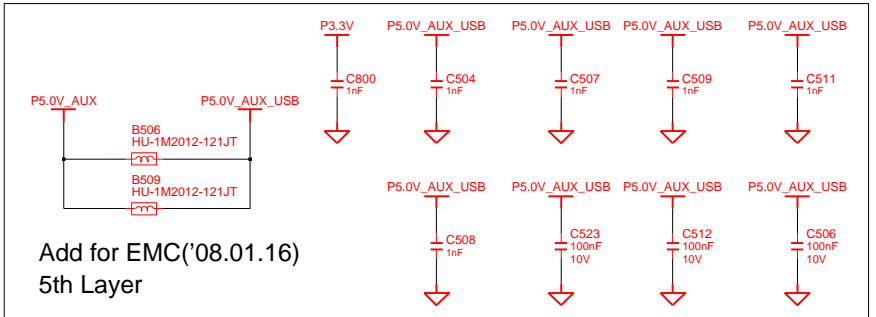
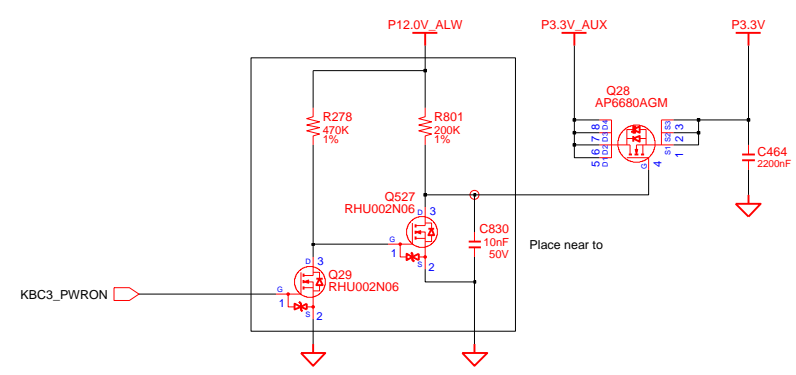


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MODULE CODE	undef ined	LAST EDIT	June 09, 2008 11:54:01 AM			
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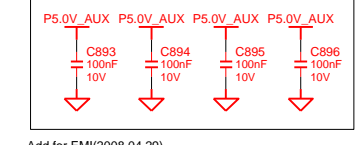
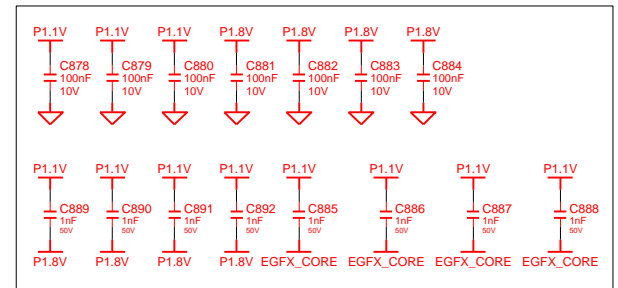
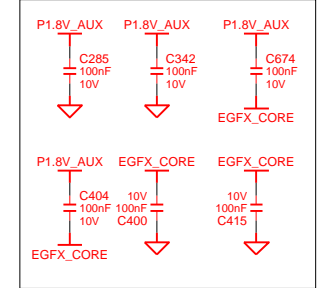
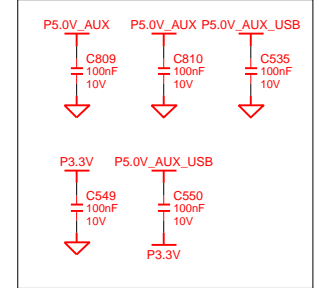
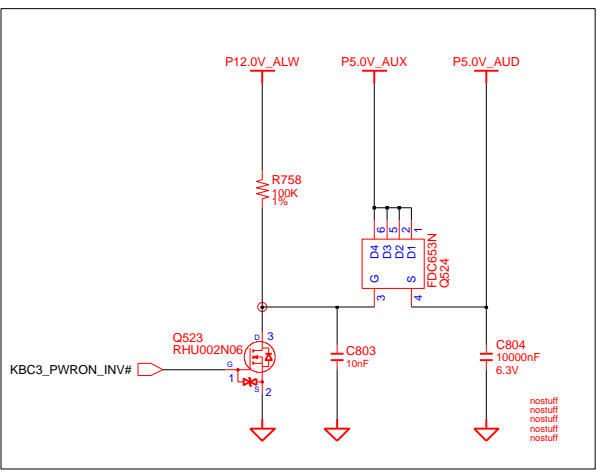
Switched Power On (P5.0V)



Switched Power On (P3.3V & 1.8V)

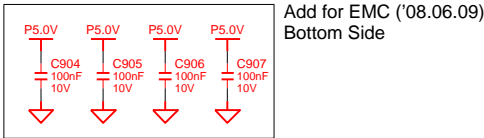
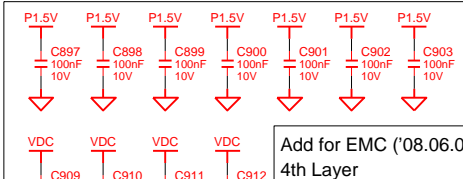
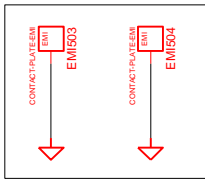
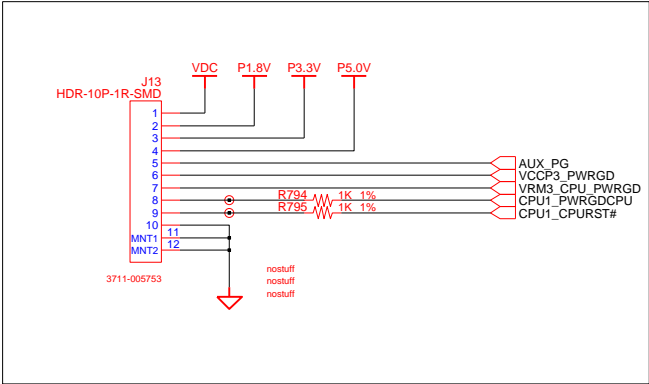


Audio Power (nostuff)

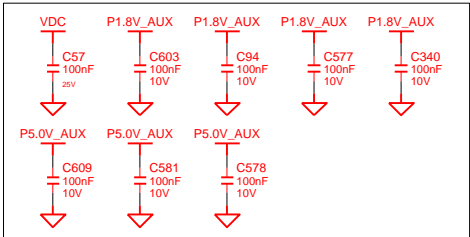
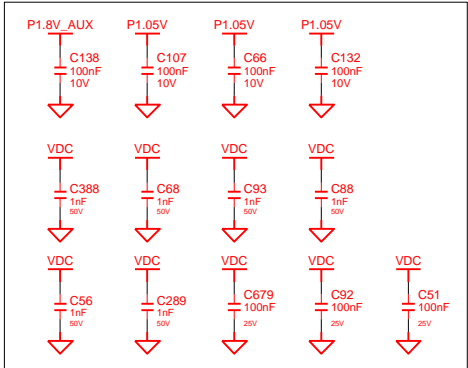
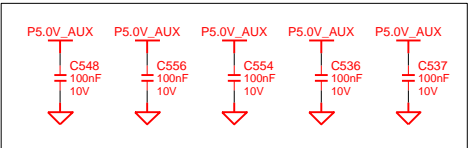
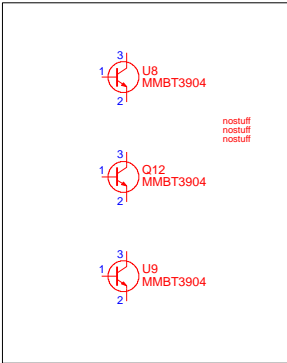


DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	MAIN		ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	MICOM & SWITCHED POWER	PART NO.	BA41-00920A
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	15	OF 19

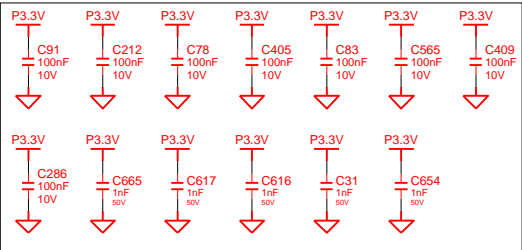
ICT PORT



For Debugging

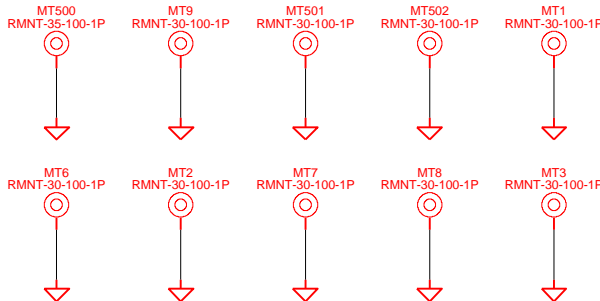


Add for EMC ('08.01.16)
Bottom Side

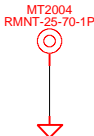


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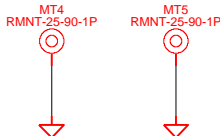
System



Board



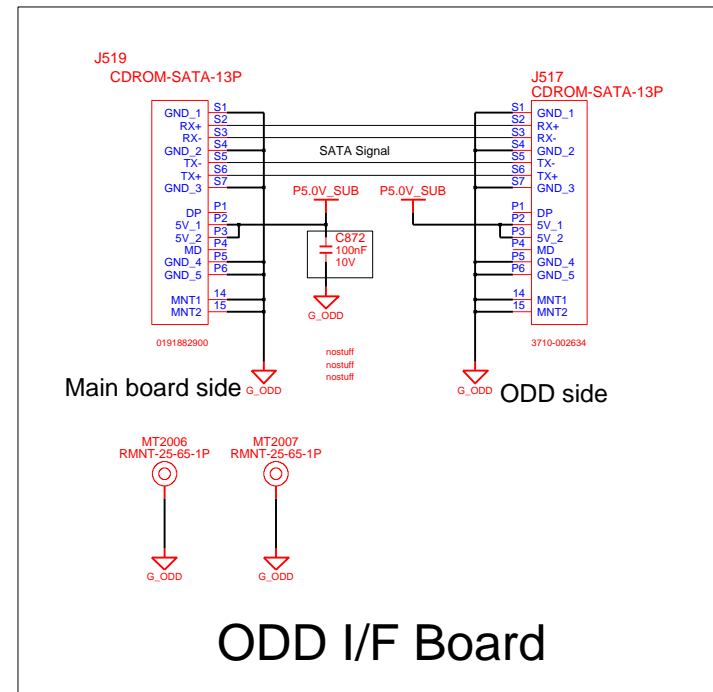
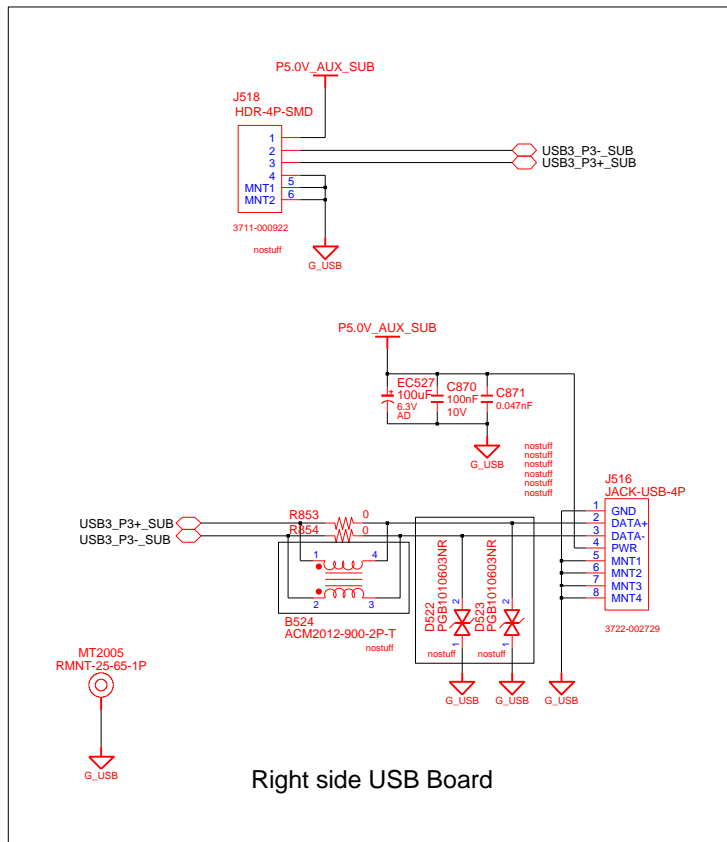
Keyboard



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP			ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	ICT PORT		PART NO. BA41-00920A
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	16	OF 19

DRAW	TERM1	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM				
				TP	PART NO.	BA41-00920A	
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Sub Board (Istanbul only)



DESIGN	TERMI	DATE	3/28/2008	TITLE	LYON_External SUB BOARD USB, ODD	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00920A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	18	OF 19

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CPU1_IGMNE#
 CPU1_VID(0)
 CPU1_VID(1)
 CPU1_VID(2)
 CPU1_VID(3)
 CPU1_VID(4)
 CPU1_VID(5)
 CPU1_VID(6)
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 EXP1_VREF
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 CPU1_VREF#
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 KBK3_PRCHEG
 KBK3_PWRSW#
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 KBK3_RFF1#
 KBK3_SMLCLK
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[illegible]

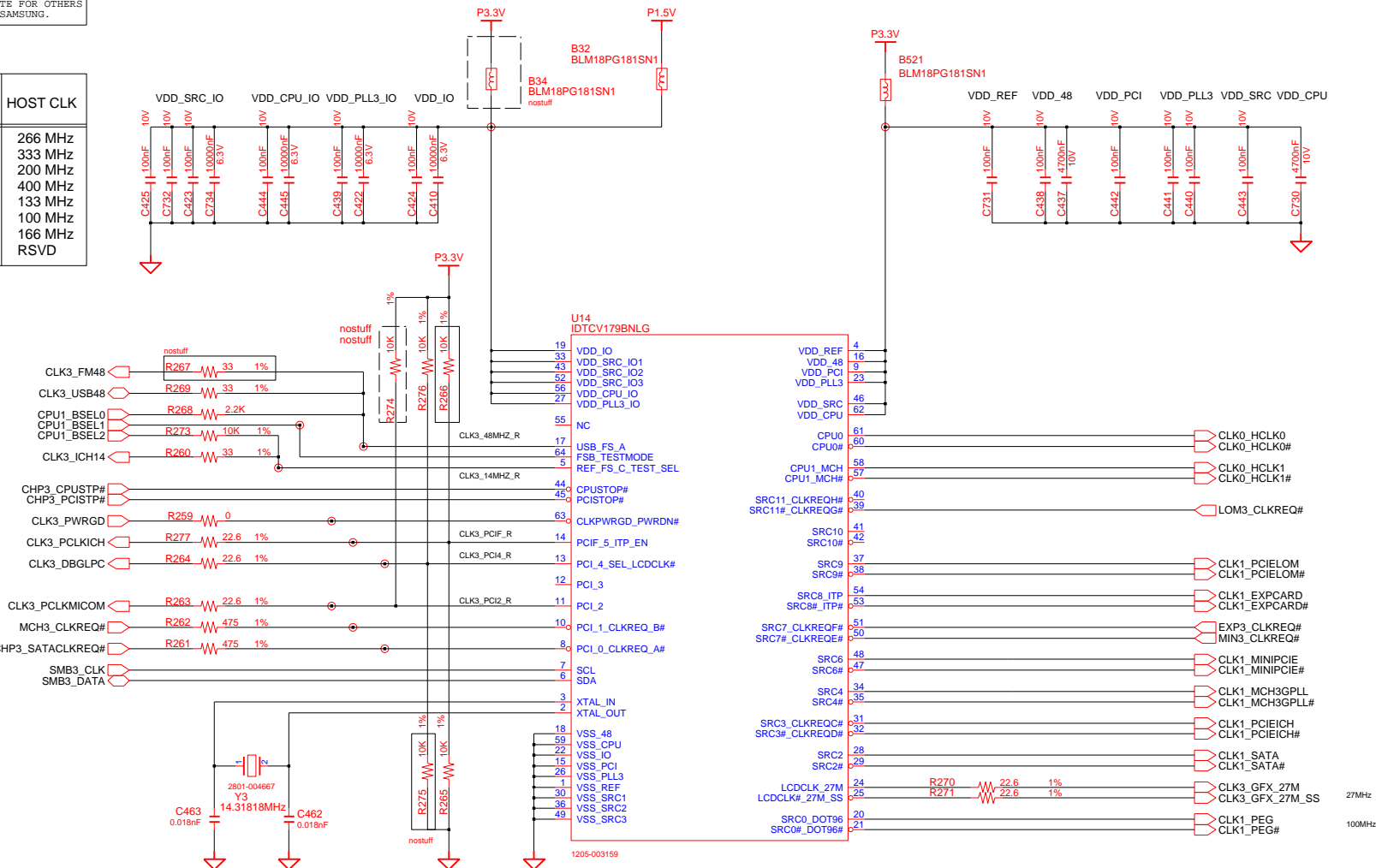
○CHP3_SUBSTA_TK
 ○PEGS_HDM_CLK
 ○MCB3_ICH5YNCI
 ○CHP3_BATACLRQEN
 ○KBC3_LED_PWRSW#
 ○KBC3_LED_POWER#
 ○KBC3_PWIRON_IN#
 ○AUD5_LIN_O_LEFT
 ○CHP3_BATACLRQEN
 ○KBC3_LED_CHARGE#
 ○KBC3_THERM_SMCLK
 ○AUD5_OUT_O_RIGHT
 ○VRMS_LDN_PWRGD
 ○AUD5_HP_O_RIGHT
 ○AUD5_MIC1_RIGHT
 ○CHP3_ME_RTCSRST#
 ○PEGS_HDM_DATA
 ○KBC3_THERM_SMDATA
 ○AUD5_MIC1_VREF_LEFT
 ○AUD5_MIC1_VREF_RIGHT
 ○P3.V3V_AUX
 ○P3.V3V_AUX
 ○P3.V3V_AUX
 ○P3.V3V_AUX
 ○VCC_CRT
 ○VDC_CHG
 ○VDC_INV
 ○VDC_INV
 ○VDC_INV
 ○VDC_INV
 ○VDC_ADPST
 ○P3.V3V_AUX_EXP
 ○P1.P1W_P2.S1_LAN
 ○VDC_VDC
 ○VDC_VDC
 ○VDC_VDC
 ○VDC_VDC
 ○VREF_VREF
 ○VREF_VREF
 ○VREF_VREF
 ○V5VFLT
 ○P3.V3V_MICOM
 ○P4.P75V_AUD

Ⓢ PS5.0V_AUX
 Ⓢ PS5.0V_AUX
 Ⓢ PS5.0V_AUX
 Ⓢ PS5.0V_AUX
 Ⓢ P1.05V_PEG
 Ⓢ P12.0V_ALW
 Ⓢ CPU_CORE
 Ⓢ CPU_CORE
 Ⓢ CPU_CORE
 Ⓢ CPU_CORE
 Ⓢ G_AUD
 Ⓢ G_CHG
 Ⓢ G_CPU
 Ⓢ G_DOR
 Ⓢ G_MIC
 Ⓢ G_GROUND
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 Ⓢ G_GROUND
 Ⓢ G_GROUND
 Ⓢ G_GROUND
 Ⓢ G_GROUND
 Ⓢ G_P3.3V
 Ⓢ G_P1.05V
 Ⓢ G_LCD_VDD3V3
 Ⓢ P0.9V
 Ⓢ P0.9V
 Ⓢ P0.9V
 Ⓢ P0.9V
 Ⓢ P1.1V
 Ⓢ P1.1V
 Ⓢ P1.1V
 Ⓢ P1.1V
 Ⓢ P3.3V
 Ⓢ P3.3V
 Ⓢ P3.3V
 Ⓢ P3.3V
 Ⓢ P5.0V
 Ⓢ P5.0V
 Ⓢ P5.0V
 Ⓢ P5.0V
 Ⓢ P1.05V
 Ⓢ P1.05V
 Ⓢ P1.05V
 Ⓢ P1.05V
 Ⓢ P1.05V
 Ⓢ PRTC_BAT

- TP2517  P1.2V_LAN
- TP2525  P1.2V_LAN
- TP2512  P1.2V_LAN
- TP2516  P1.2V_LAN
- TP2517  P1.5V
- TP2525  P1.5V
- TP2516  P1.5V
- TP2517  P1.5V_EXP
- TP2525  P1.5V_EXP
- TP2516  P1.5V_EXP
- TP2517  P1.8V_AUX
- TP2525  P1.8V_AUX
- TP2516  P1.8V_AUX
- TP2517  P3.3V_EXP
- TP2525  P3.3V_MCD
- TP2516  P5.0V_ALW
- TP2517  P5.0V_AUD
- TP2525  P5.0V_AMP
- TP2516  P5.0V_AUX_USB
- TP2506  EGFX_CORE
- TP2507  EGFX_CORE
- TP2508  EGFX_CORE
- TP2504  EGFX_CORE
- TP2505  P1.8V
- TP2502  P1.8V
- TP2503  P1.8V
- TP2509  P1.8V

DESIGN	TERM1	DATE	1/10/2008	LYON_External TP UNDEF INED	SAMSUNG ELECTRONICS		
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0			PART NO.	BA41-00920A
MODULE CODE	LAST EDIT		June 09, 2008 11:54:01 AM			PAGE 19 OF 19	

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

IDT : 1205-003159
Silego : 1205-003156
Spectra Linear : 1205-003533

This part is 64pin QFN package.

DRAW	TERM1	DATE	1/10/2008	TITLE	LYON_External Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM				PAGE

The diagram illustrates the electrical connections for the CPU board, focusing on power, ground, and signal lines. Key components and connections include:

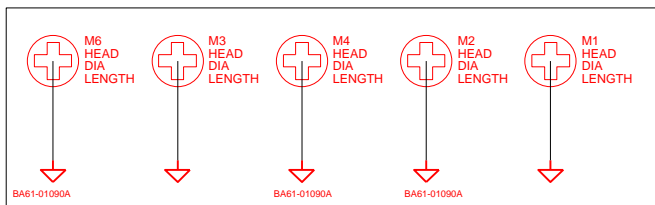
- Power and Ground:**
 - P5.0V:** Connected to C64 (1000nF, 6.3V) and C82 (100nF, 10V).
 - P3.3V_AUX:** Connected to R53 (49.9Ω) and C79 (100nF, 10V).
 - P3.3V:** Connected to R55, R57, R56, and R70 (all 10KΩ, 1%).
 - P3.3V_AUX:** Connected to R70 (10KΩ, 1%).
- Signal and Control:**
 - U7 EMC2102:** A temperature sensor with pins 1, 24, 27, 14, 16, 10, 25, 26, 13, 9, 11, 8, 15, and 21.
 - TP2472:** A 93 degree C temperature sensor with pins 1, 2, and 3.
 - TP2477:** A 93 degree C temperature sensor with pins 1, 2, and 3.
 - TP2473:** A 93 degree C temperature sensor with pins 1, 2, and 3.
 - TP2475:** A 93 degree C temperature sensor with pins 1, 2, and 3.
 - TP2476:** A 93 degree C temperature sensor with pins 1, 2, and 3.
- Other Components:**
 - R68:** 200KΩ, 1%.
 - R69:** 61.1KΩ, 1%.
 - R71:** 20KΩ, 1%.
 - R72:** 20KΩ, 1%.
 - R73:** 20KΩ, 1%.
 - R74:** 20KΩ, 1%.
 - R75:** 20KΩ, 1%.
 - R76:** 20KΩ, 1%.
 - R77:** 20KΩ, 1%.
 - R78:** 20KΩ, 1%.
 - R79:** 20KΩ, 1%.
 - R80:** 20KΩ, 1%.
 - R81:** 20KΩ, 1%.
 - R82:** 20KΩ, 1%.
 - R83:** 20KΩ, 1%.
 - R84:** 20KΩ, 1%.
 - R85:** 20KΩ, 1%.
 - R86:** 20KΩ, 1%.
 - R87:** 20KΩ, 1%.
 - R88:** 20KΩ, 1%.
 - R89:** 20KΩ, 1%.
 - R90:** 20KΩ, 1%.
 - R91:** 20KΩ, 1%.
 - R92:** 20KΩ, 1%.
 - R93:** 20KΩ, 1%.
 - R94:** 20KΩ, 1%.
 - R95:** 20KΩ, 1%.
 - R96:** 20KΩ, 1%.
 - R97:** 20KΩ, 1%.
 - R98:** 20KΩ, 1%.
 - R99:** 20KΩ, 1%.
 - R100:** 20KΩ, 1%.

10mil width and 10mil spacing.

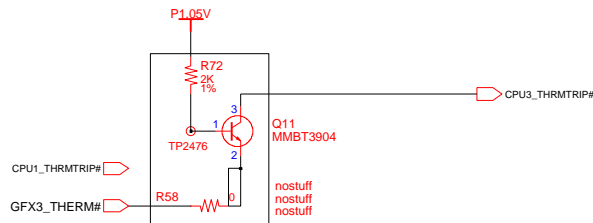
Opposite side of CPU.

Line Width = 20 mil

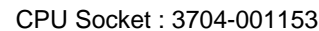
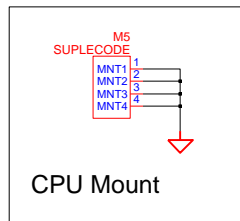
RHE Support (Top)



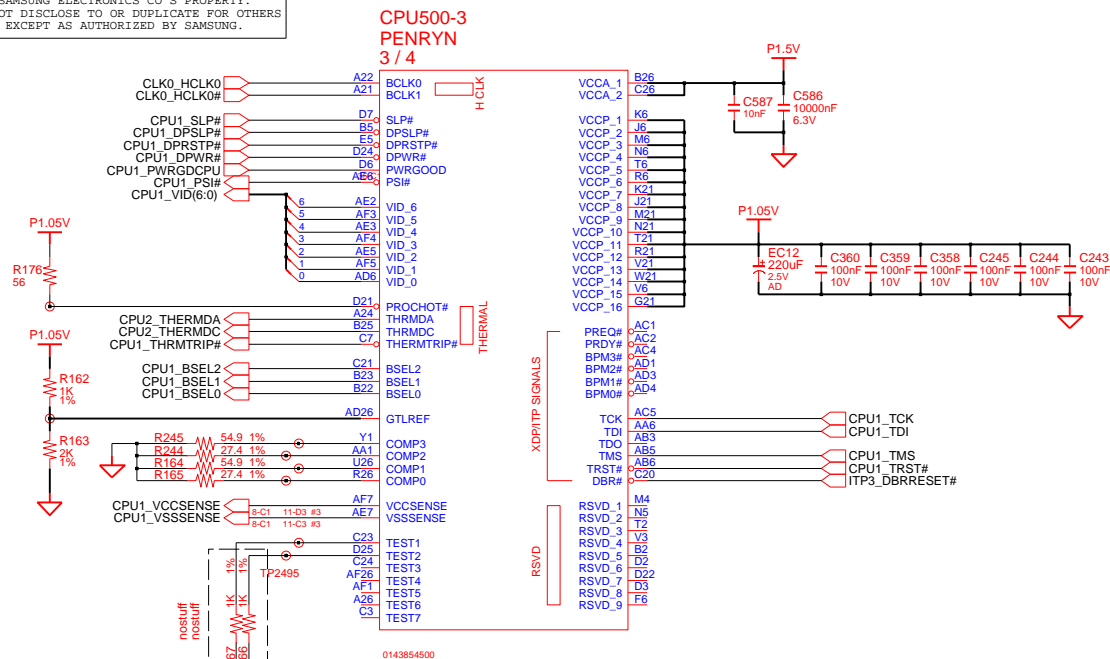
M6
Internal : nostuff
External : stuff



DRAW	TERM1	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG	
CHECK	HJ KIM	DEV. STEP	MP	Thermal_Sensor_SMSC_Emc2102	ELECTRONICS		
APPROVAL	SJ PARK	REV	1.0	Thermal_Sensor_SMSC_Emc2102	PART NO.	BA41-00920A	
MODULE CODE	LAST EDIT		June 09, 2008 11:54:01 AM		PAGE	61	OF 64



DRAM	TERM1	DATE	1/10/2008	LYON_External CPU PENRYN (1/3)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM		



CPU Socket : 3704-001153

FSC	FSB	FSA	FRQ
0	0	0	266M
0	1	0	200M
0	1	1	166M

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6.0)	Voltage	VID(6.0)	Voltage	VID(6.0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0 0	1.0000 V	1 0 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0 1	0.9875 V	1 0 1 1 0 0 0 1	0.4750 V
0 0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 0 1	0.9625 V	1 0 1 0 1 0 0 0	0.4500 V
0 0 0 0 0 1 0 0	1.4500 V	0 1 0 1 0 1 0 0	0.9500 V	1 0 1 0 1 0 0 1	0.4375 V
0 0 0 0 0 1 0 1	1.4375 V	0 1 0 1 0 1 0 1	0.9375 V	1 0 1 1 0 0 0 0	0.4250 V
0 0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0 0	0.9250 V	1 0 1 0 1 0 1 1	0.4125 V
0 0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1 1	0.9125 V	1 0 1 1 1 0 0 0	0.4000 V
0 0 0 0 1 0 0 0	1.4000 V	0 1 1 1 0 0 0 0	0.9000 V	1 0 1 1 1 0 0 1	0.3875 V
0 0 0 0 1 0 0 1	1.3875 V	0 1 1 1 0 0 0 1	0.8875 V	1 0 1 1 1 0 1 0	0.3750 V
0 0 0 0 1 0 1 0	1.3750 V	0 1 1 1 0 0 1 0	0.8750 V	1 0 1 1 1 0 1 1	0.3625 V
0 0 0 0 1 0 1 1	1.3625 V	0 1 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 1 0 0	0.3500 V
0 0 0 0 1 1 0 0	1.3500 V	0 1 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 1 0 1	0.3375 V
0 0 0 0 1 1 0 1	1.3375 V	0 1 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 1 0	0.3250 V
0 0 0 0 1 1 0 1	1.3250 V	0 1 1 1 0 1 0 1	0.8250 V	1 0 1 1 1 1 1 1	0.3125 V
0 0 0 0 1 1 1 0	1.3125 V	0 1 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0 0	0.3000 V
0 0 0 0 1 1 0 0	1.3000 V	0 1 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 0 1	0.2875 V
0 0 0 0 1 1 0 0	1.2875 V	0 1 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 0 1 0	0.2750 V
0 0 0 0 1 1 0 0	1.2750 V	0 1 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 0 1 1	0.2625 V
0 0 0 0 1 1 0 0	1.2625 V	0 1 1 1 1 0 1 0	0.7625 V	1 1 0 0 0 1 0 0	0.2500 V
0 0 0 0 1 1 0 0	1.2500 V	0 1 1 1 1 1 0 0	0.7500 V	1 1 0 0 0 1 0 1	0.2375 V
0 0 0 0 1 1 0 1	1.2375 V	0 1 1 1 1 1 0 1	0.7375 V	1 1 0 0 0 1 1 0	0.2250 V
0 0 0 0 1 1 0 1	1.2250 V	0 1 1 1 1 1 1 0	0.7250 V	1 1 0 0 0 1 1 1	0.2125 V
0 0 0 0 1 1 1 0	1.2125 V	0 1 1 1 1 1 1 1	0.7125 V	1 1 0 0 1 0 0 0	0.2000 V
0 0 0 0 1 1 1 0	1.2000 V	1 0 0 0 0 0 0 0	0.7000 V	1 1 0 0 1 0 0 1	0.1875 V
0 0 0 0 1 1 1 0	1.1875 V	1 0 0 0 0 0 0 1	0.6875 V	1 1 0 0 1 0 1 0	0.1750 V
0 0 0 0 1 1 1 0	1.1750 V	1 0 0 0 0 0 1 0	0.6750 V	1 1 0 0 1 0 1 1	0.1625 V
0 0 0 0 1 1 1 0	1.1625 V	1 0 0 0 0 0 1 1	0.6625 V	1 1 1 1 0 0 0 0	0.1500 V
0 0 0 0 1 1 1 0	1.1500 V	1 0 0 0 0 0 1 1	0.6500 V	1 1 1 1 0 0 0 1	0.1375 V
0 0 0 0 1 1 1 0	1.1375 V	1 0 0 0 0 0 1 1	0.6375 V	1 1 1 0 1 1 1 0	0.1250 V
0 0 0 0 1 1 1 1	1.1250 V	1 0 0 0 0 0 1 1	0.6250 V	1 1 1 0 1 1 1 1	0.1125 V
0 0 0 0 1 1 1 1	1.1125 V	1 0 0 0 0 0 1 1	0.6125 V	1 1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0 0	1.1000 V	1 0 0 0 0 0 1 1	0.6000 V	1 1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 0 0	1.0875 V	1 0 0 0 0 0 1 1	0.5875 V	1 1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 0 0 1	1.0750 V	1 0 0 0 0 1 0 0	0.5750 V	1 1 1 0 0 0 0 1	0.0625 V
0 1 0 0 0 0 0 1	1.0625 V	1 0 0 0 0 1 0 0	0.5625 V	1 1 1 1 0 0 0 0	0.0500 V
0 1 0 0 0 0 0 1	1.0500 V	1 0 0 0 0 1 0 0	0.5500 V	1 1 1 1 0 0 0 1	0.0375 V
0 1 0 0 0 0 1 0	1.0375 V	1 0 0 0 0 1 0 0	0.5375 V	1 1 1 1 0 0 1 0	0.0250 V
0 1 0 0 0 0 1 0	1.0250 V	1 0 0 0 0 1 0 0	0.5250 V	1 1 1 1 0 0 1 1	0.0125 V
0 1 0 0 0 0 1 1	1.0125 V	1 0 0 0 0 1 1 1	0.5125 V	1 1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 0 0 0 0	0.5000 V	1 1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V

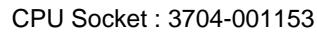
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with $Z_0=55\text{ohm}$ trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with $Z_0=27.4\text{ohm}(55\text{ohm})$ trace shorter than $1/2"$ to their respective Banias socket pins.

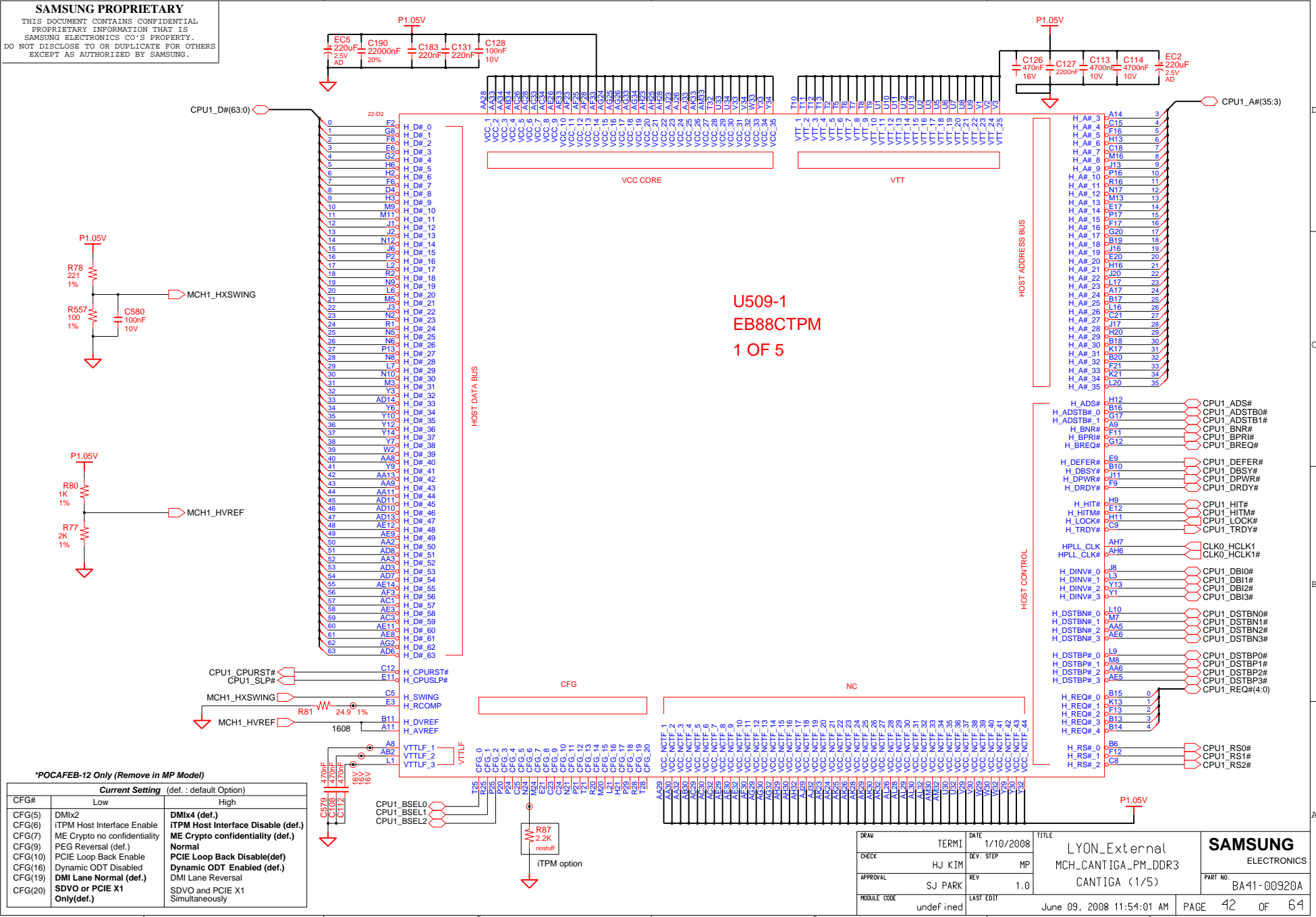
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a $Z_0=55\text{ohm}$ traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

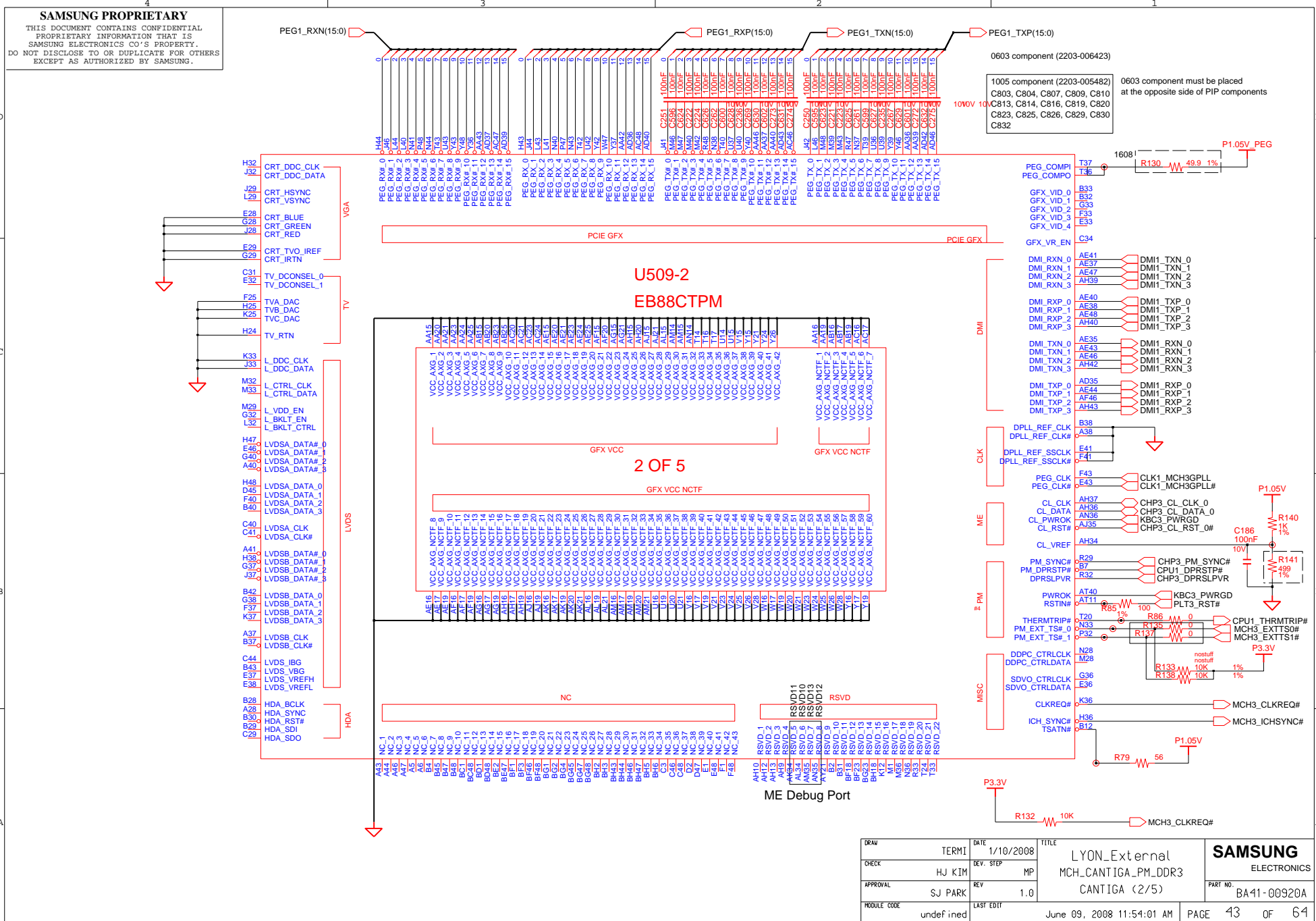
DRAM	TERM1	DATE	1/10/2008	LYON_External CPU PENRYN (2/3)	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP		PART NO. BA41-00920A	
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM			PAGE

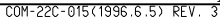


DRAM	TERM1	DATE	1/10/2008	TITLE	LYON_External CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK	HJ KM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT				
				June 09, 2008 11:54:01 AM	PAGE	24 OF 64

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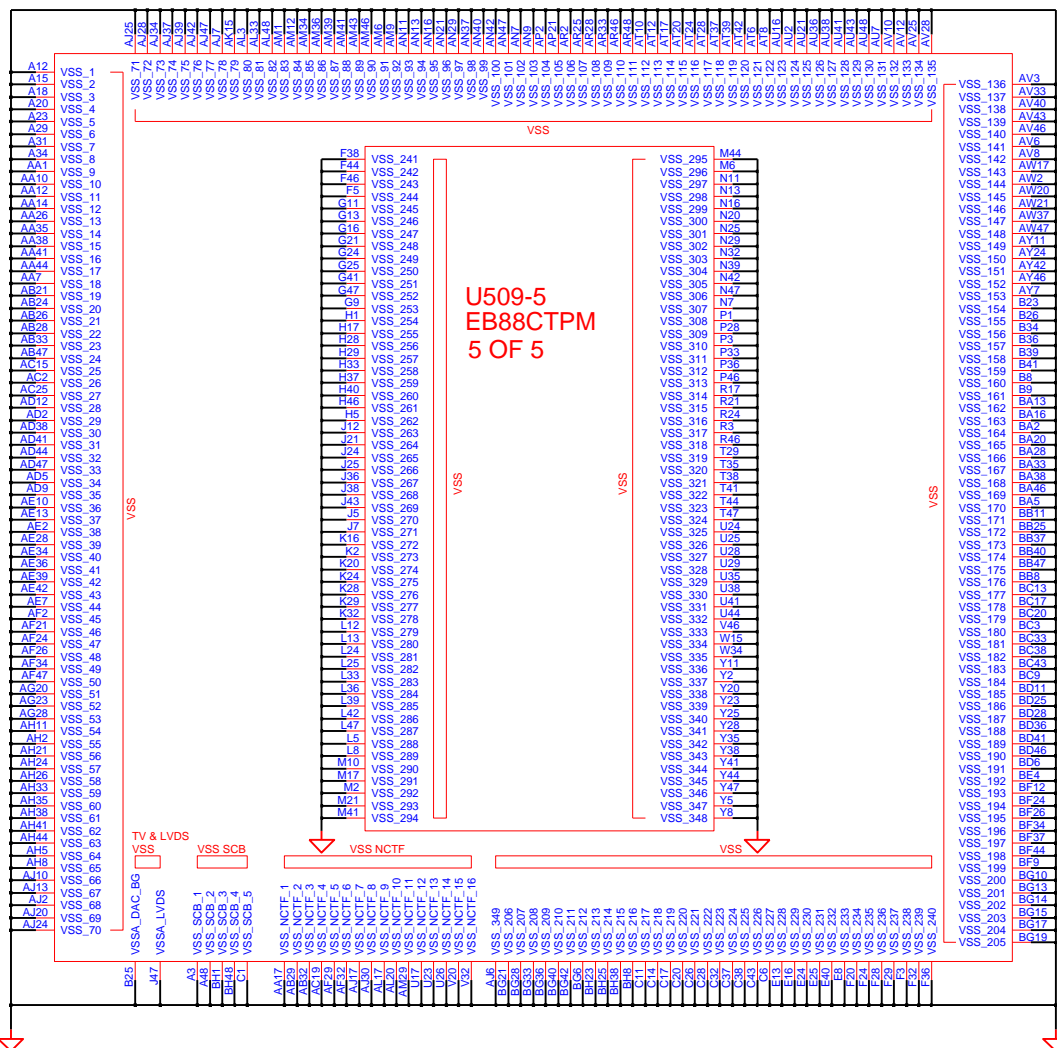






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DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	MCH_CANTIGA_PM_DDR3	ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0	CANTIGA (5/5)	PART NO.	BA41-00920A
MODULE CODE	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	46	OF	64

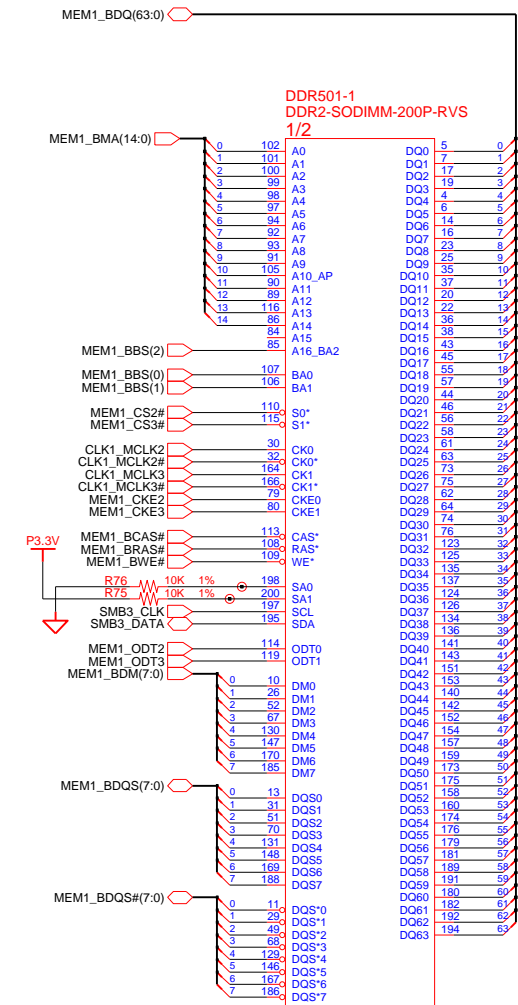
DDR SO-DIMM #1
Height : 9.2mm (Reverse)

D

C

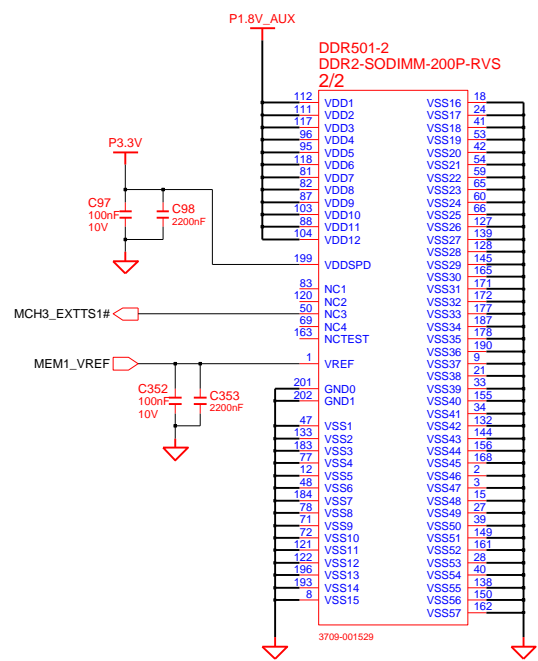
B

A

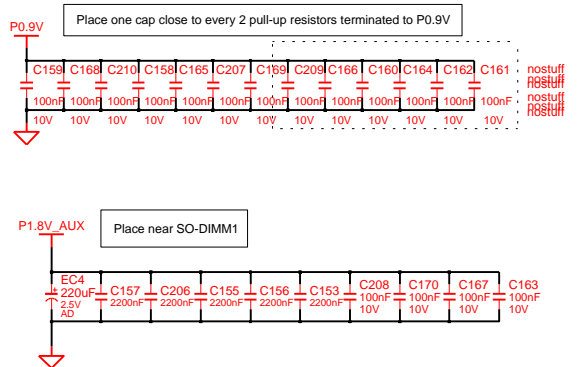
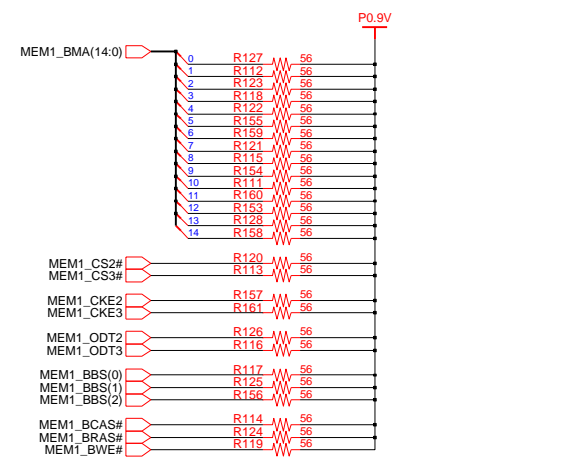


DDR501-1
DDR2-SODIMM-200P-RVS
1/2

ME POWER RAIL UNDER ME ENABLE



DDR501-2
DDR2-SODIMM-200P-RVS
2/2



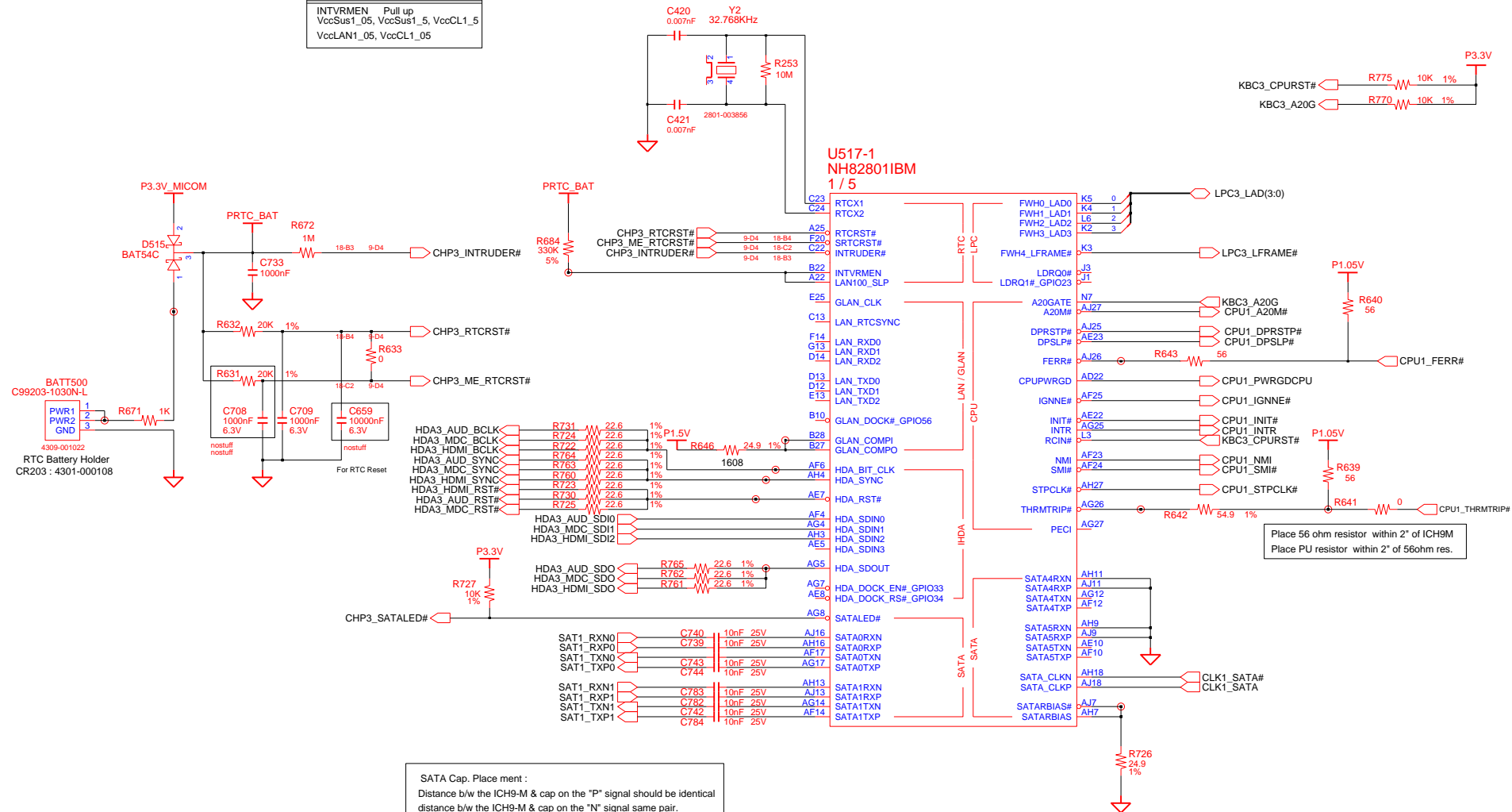
Foxcon : 3709-001529
Suyin : 3709-001503

DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		SODIMM_DDR2	
APPROVAL	SJ PARK	REV	1.0		SODIMM_DDR2 #2	PART NO. BA41-00920A
MODULE CODE		LAST EDIT				

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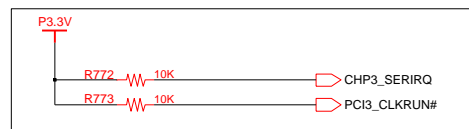
Internal VR Strap	
INTVRMEN	Pull up
VccSus1_05, VccSus1_5, VccCL1_5	
VccLAN1_05, VccCL1_05	



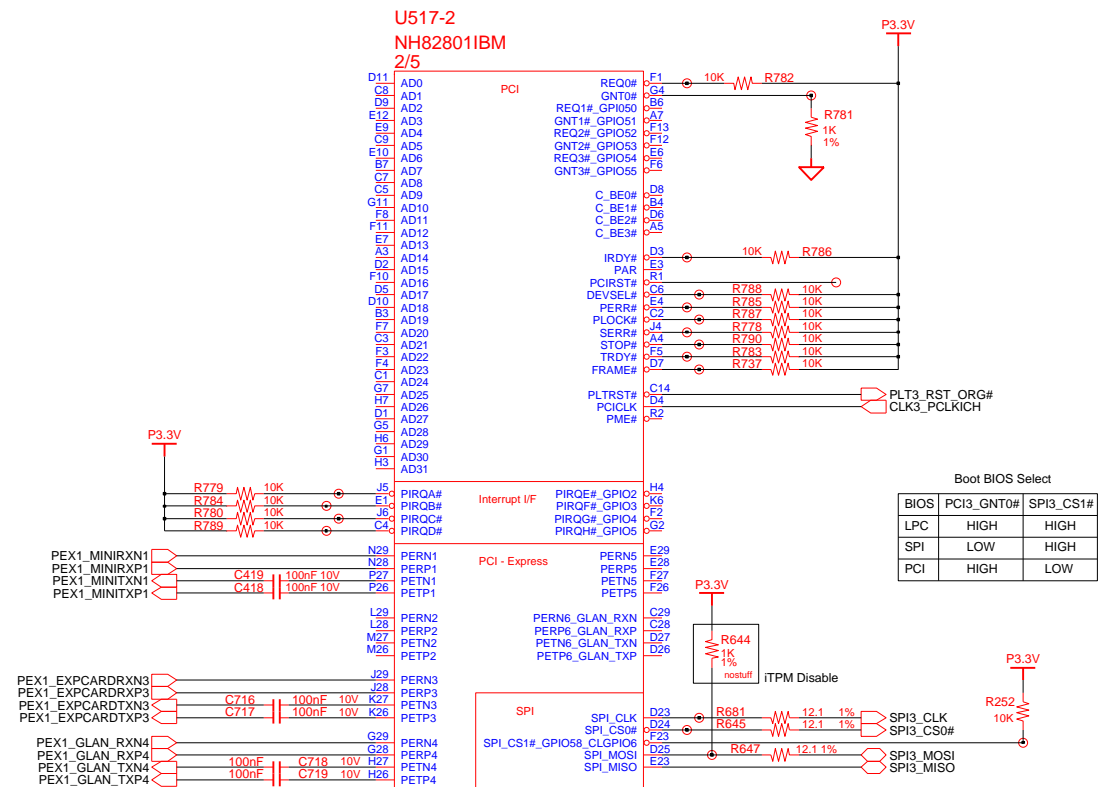
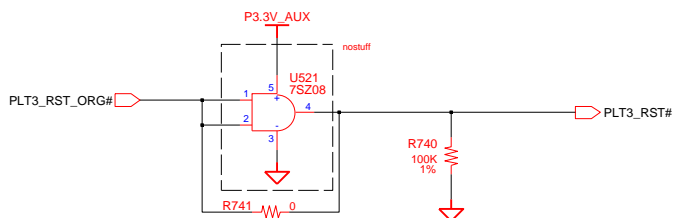
SATA Cap. Place ment :
Distance b/w the ICH9-M & cap on the "P" signal should be identical
distance b/w the ICH9-M & cap on the "N" signal same pair.

Place 56 ohm resistor within 2" of ICH9M
Place PU resistor within 2" of 56ohm res.

DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP		ICH9M_B	
APPROVAL	SJ PARK	REV	1.0		ICH9-M (1/5)	
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	34 OF 64	



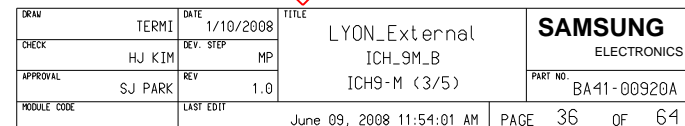
LPC option : These are used with LPC

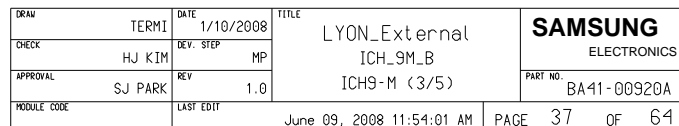


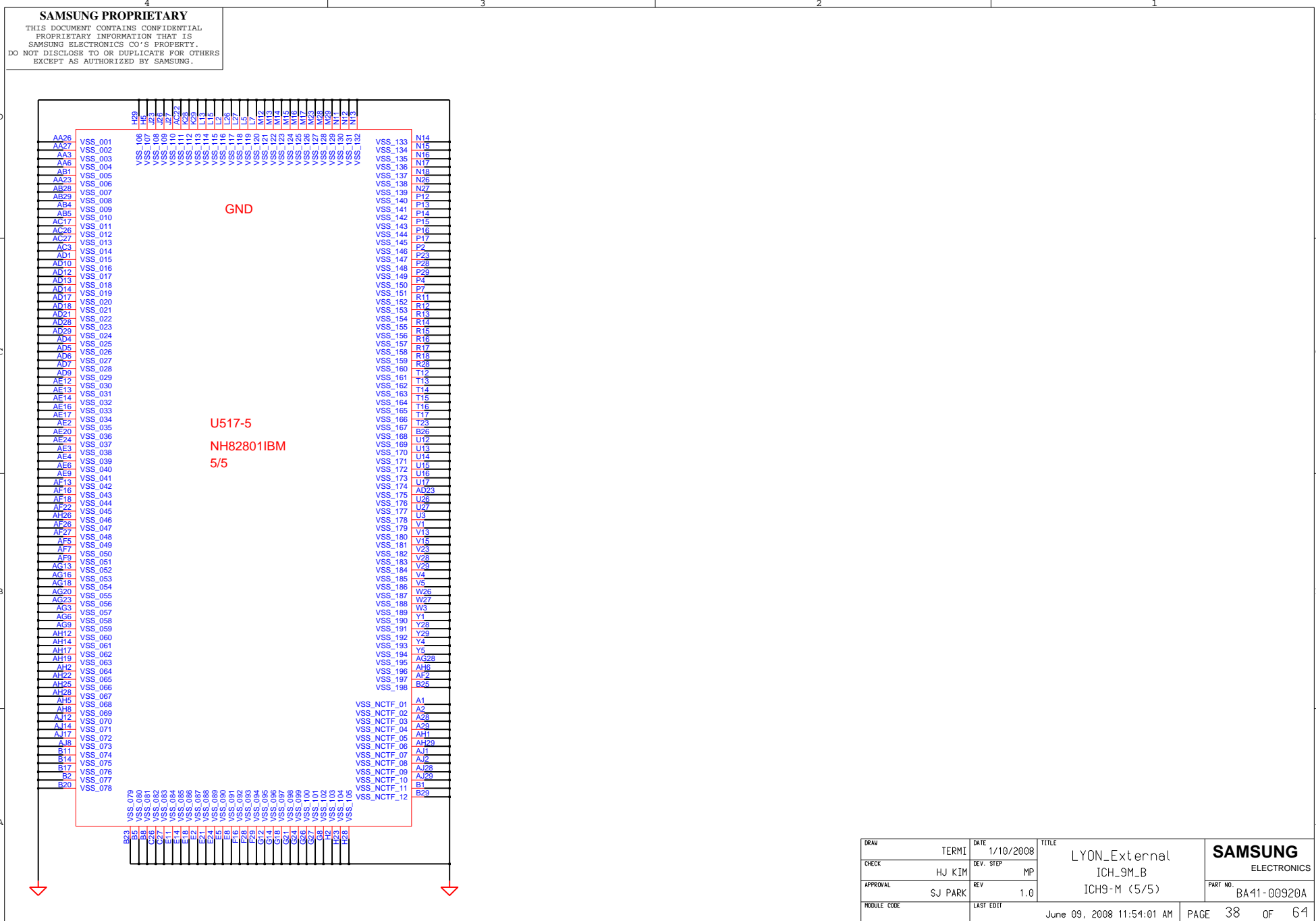
AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stufing Option to minimize stubs

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

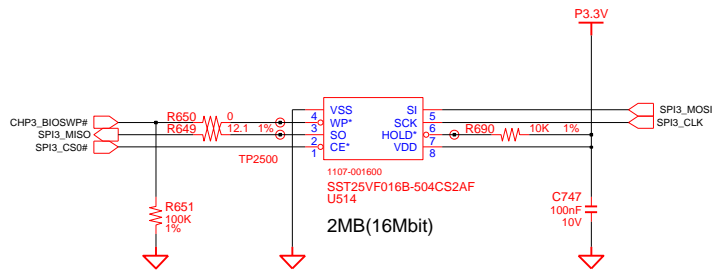
DRAM	TERM1	DATE	1/10/2008	TITLE	LYON_External ICH_9M.B ICH9-M (2/5)	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM				PAGE







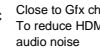
- SPI ROM LIST -



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
OE	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY * PRESS SETUP*	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

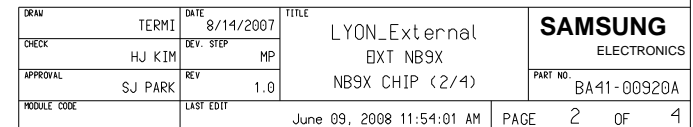
DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP		SPI_BIOS_ROM	
APPROVAL	SJ PARK	REV	1.0		SPI_BIOS_ROM	
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	60 OF 64	

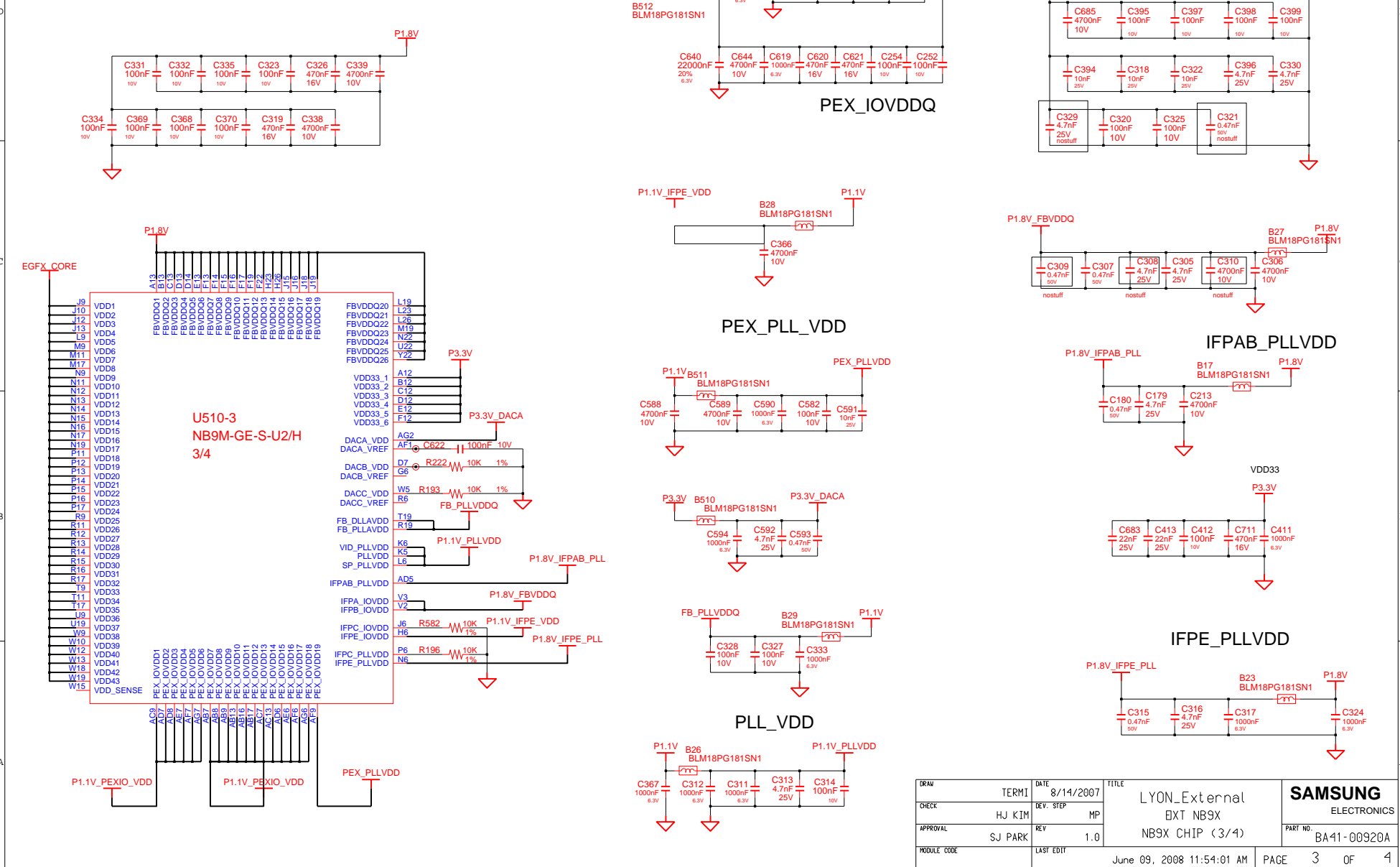
To maintain Voff voltage under 10mV by blocking current path. (2008.05.02)



D:\users\mobile62\mentor\lyon\lyon-ext_mp10_080603\design_blocks\Gfx_External_Nvidia_Nb9x_64bit

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DRAM	DATE	8/14/2007	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	TERM1	8/14/2007	LYON_External	
	DEV. STEP	MP	EXT NB9X	
APPROVAL	REV	1.0	NB9X CHIP (3/4)	
MODULE CODE	LAST EDIT	June 09, 2008 11:54:01 AM		
			PAGE	3 OF 4

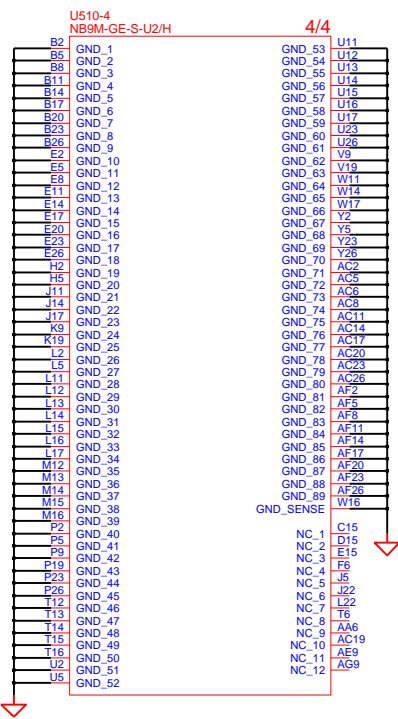
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D

C

B

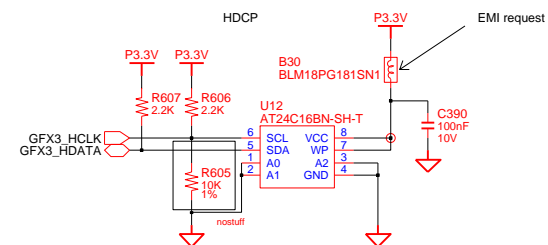
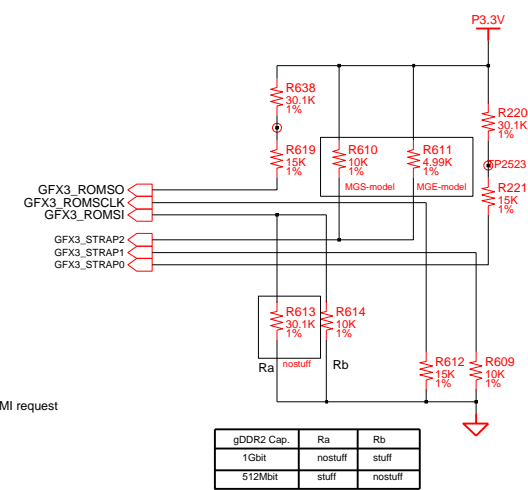
A



Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU VID1	NC
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SLU Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK27 = 1 27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP	
25K ohm	1100	0100	NB9M-GS:0x06E8 (01001)	
30K ohm	1101	0101	NB9M-GE:0x06E8 (01000)	
35K ohm	1110	0110	NB9P-GS:0x0649 (01001)	
45K ohm	1111	0111	NB9P-GE:0x0406 (00110)	
	1111	0111	NB9P-GE2:0x07?? (0????)	

	Bit3	Bit2	Bit1	Bit0
ROMSO	1	1	1	1
SCLK	0	0	1	0
SI	0	1	0	1
	0	0	0	1
	0	0	0	1
Strap2	1	0	0	1
	1	0	0	0
Strap1	0	0	0	1
Strap0	1	1	1	1



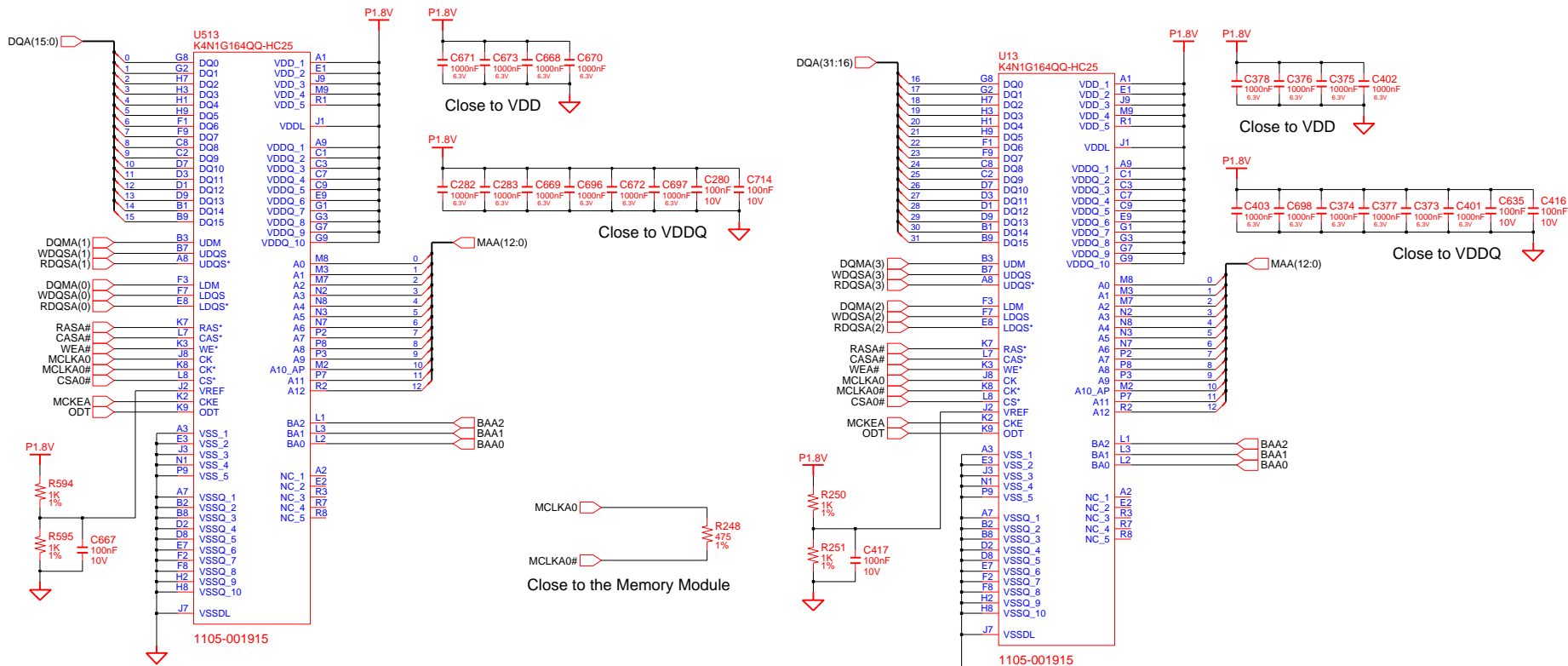
PU is for I2C ROM (AT24C16B, A0-A2 = 000)
PD is for Crypto ROM

DRAW	TERMI	DATE	8/14/2007	TITLE	LYON_External	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		BXT NB9X	
APPROVAL	SJ PARK	REV	1.0		NB9X CHIP (4/4)	
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	4 OF 4	

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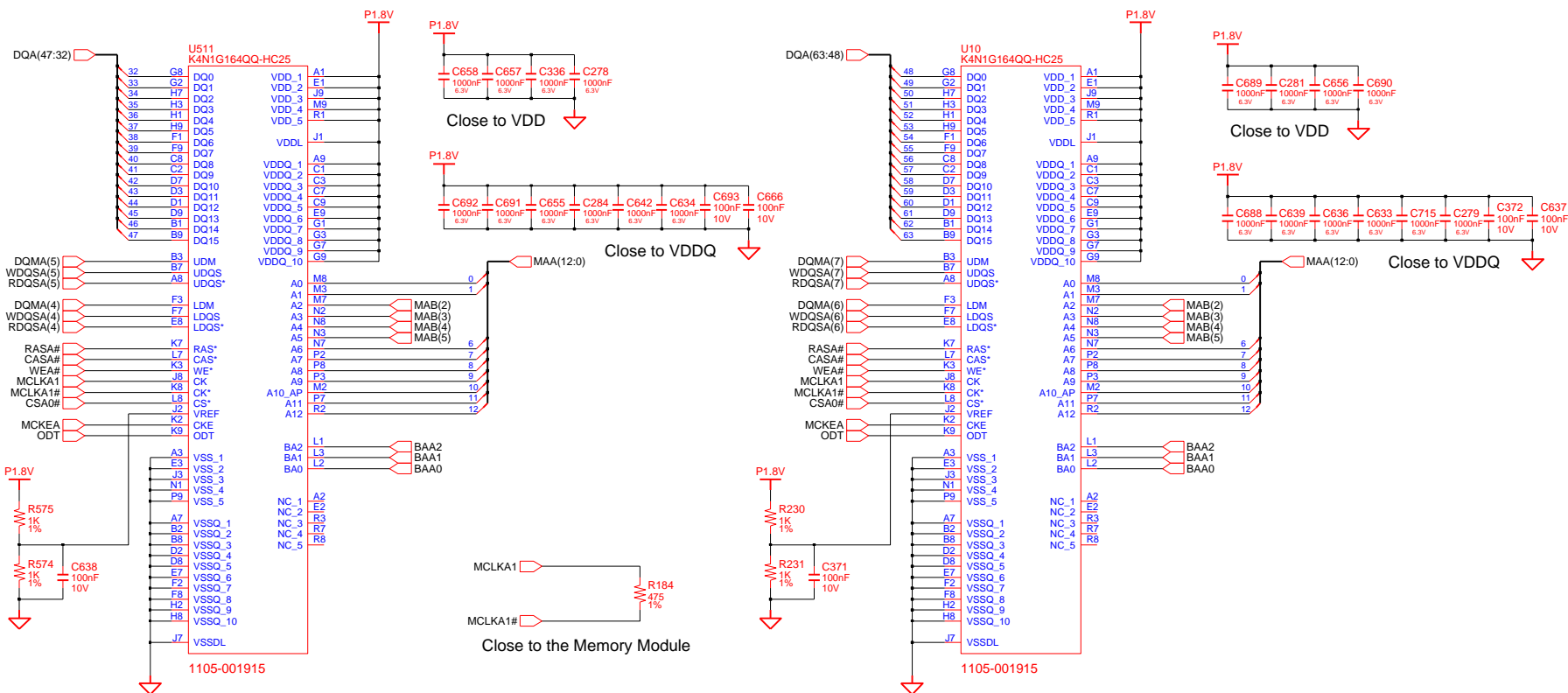
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LOWER SUB PARTITION

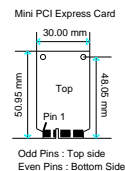


DATE	8/12/2006	TITLE	LYON_External	SAMSUNG ELECTRONICS
TERMI		DEV. STEP	MP	
CHECK	HJ KIM	REV	1.0	PART NO. BA41-00920A
APPROVAL	SJ PARK	LAST EDIT	June 09, 2008 11:54:01 AM	
MODULE CODE				PAGE 1 OF 2

UPPER SUB PARTITION



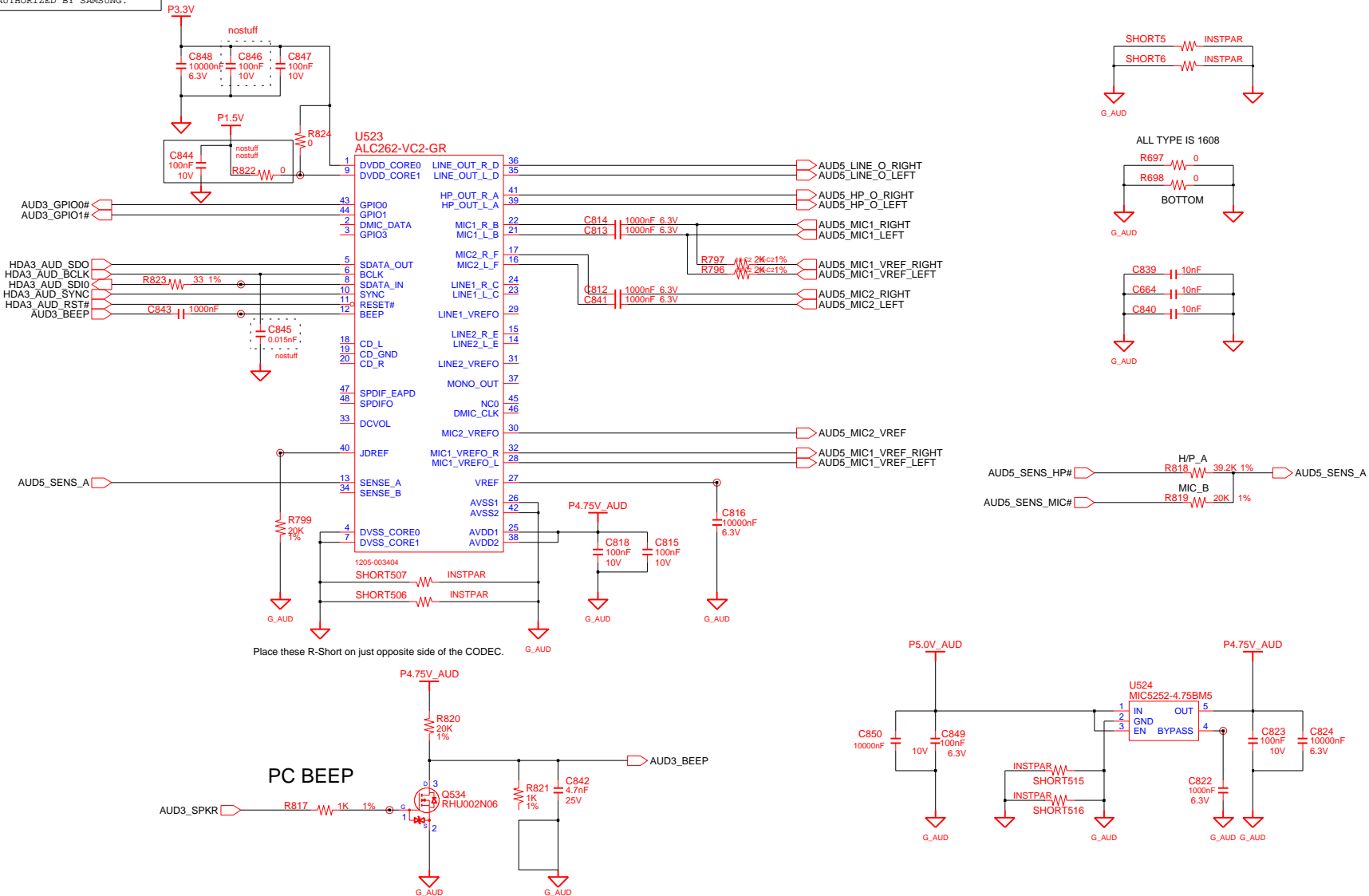
DRWN	TERMI	DATE	8/12/2006	TITLE	LYON_External		SAMSUNG	
CHECK	HJ KIM	DEV. STEP	MP		Graphics_Memory(GDDR2)		ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0		Graphics_Memory_Nvidia #2		PART NO.	BA41-00920A
MODULE CODE	LAST EDIT			June 09, 2008 11:54:01 AM		PAGE	2	OF 2



DRAW		DATE	TITLE		SAMSUNG ELECTRONICS	
TERMI		1/10/2008	LYON_External			
CHECK	HJ KIM	REV. STEP	MP	PCIE_Minicard_Slot	PART NO. BA41-00920A	
APPROVAL	SJ PARK	REV	1.0	PCIE_Minicard_Slot		
MODULE CODE		LAST EDIT			PAGE 51 OF 64	
undefined		June 09, 2008 11:54:01 AM				

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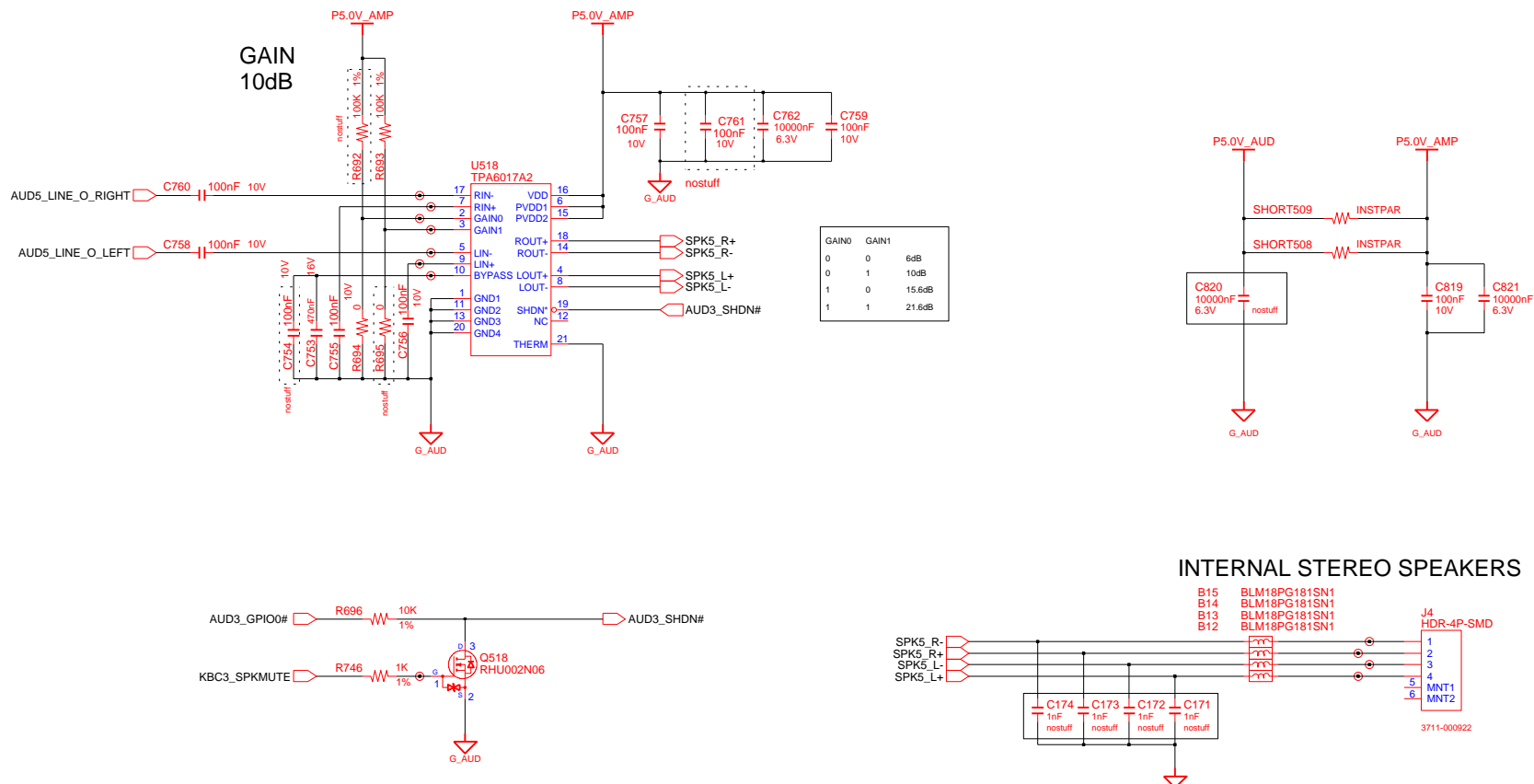
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DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	HDA_Codec_Alc262	ELECTRONICS	
APPROVAL	SJ PARK	REV	1.0	HDA_Codec_Alc262 #1	PART NO.	BA41-00920A
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	28	OF 64

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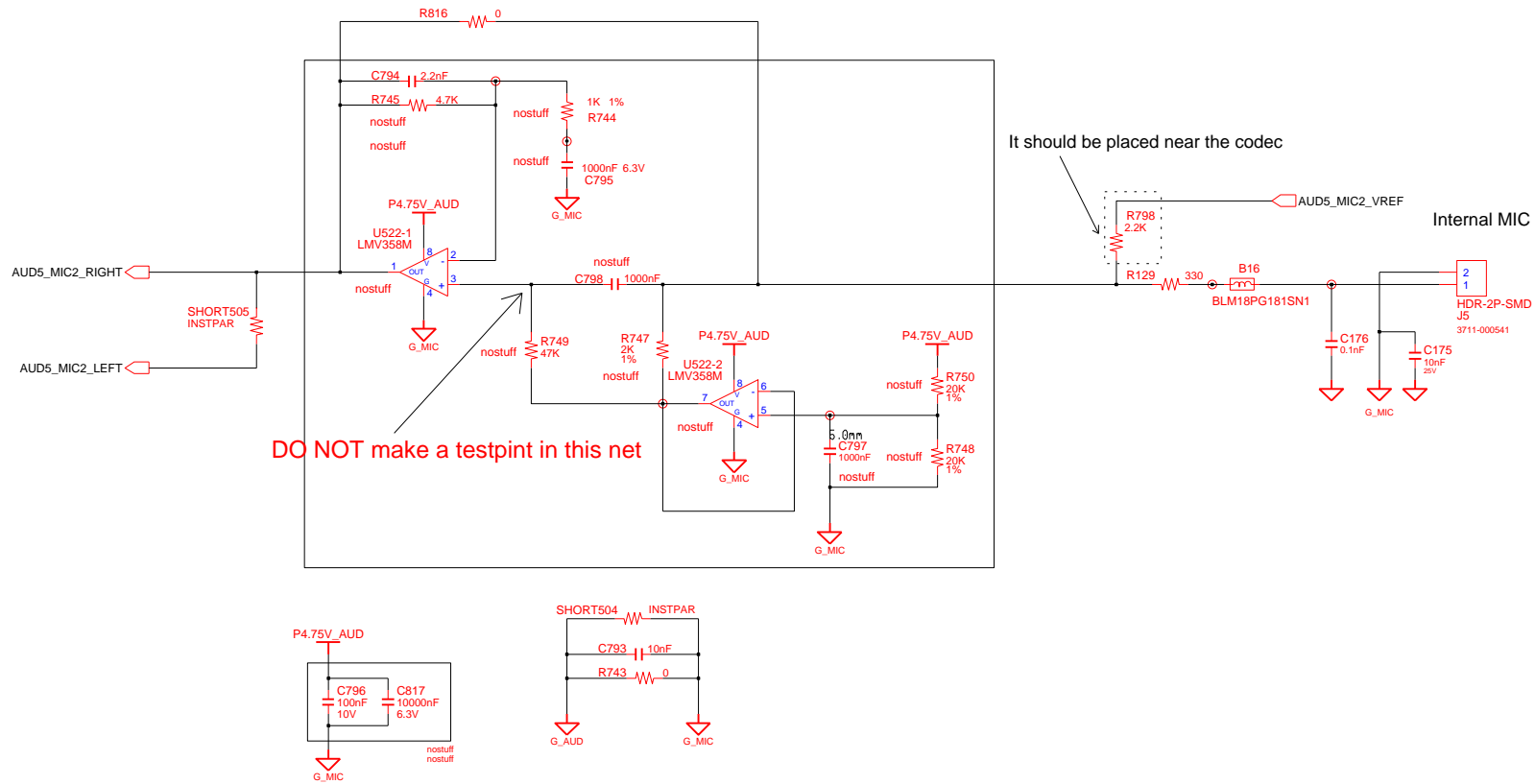
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DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	HDA_Codec_Alc262		
APPROVAL	SJ PARK	REV	1.0	HDA_Codec_Alc262 #2		
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM			
PAGE 29 OF 64						PART NO. BA41-00920A

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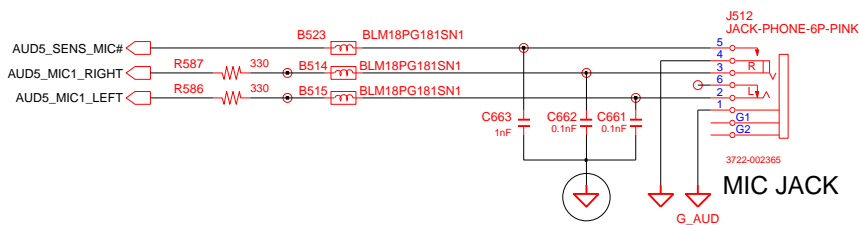
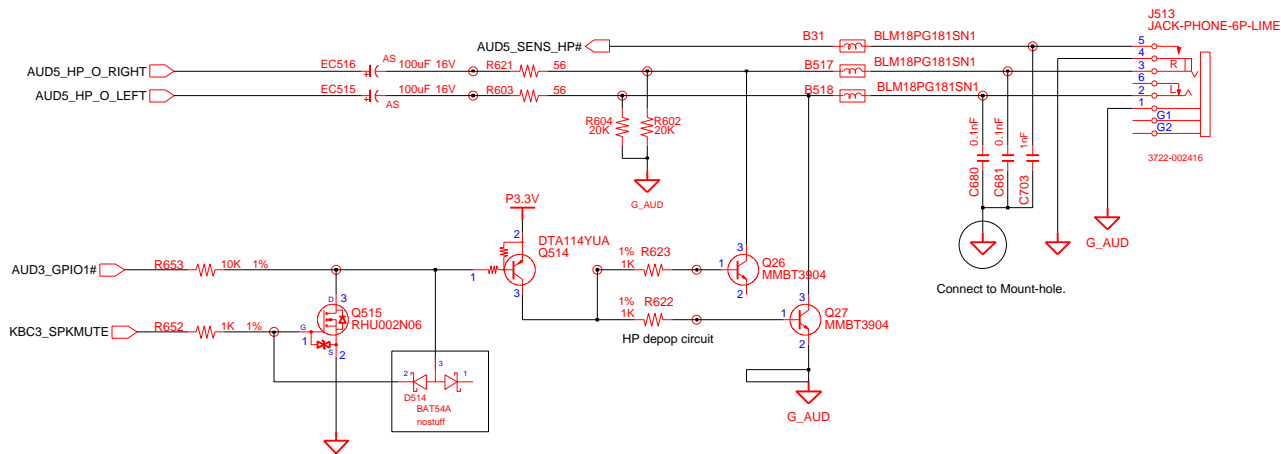


DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP		HDA_Codec_Alc262	
APPROVAL	SJ PARK	REV	1.0		HDA_Codec_Alc262 #3	
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	30 OF 64	

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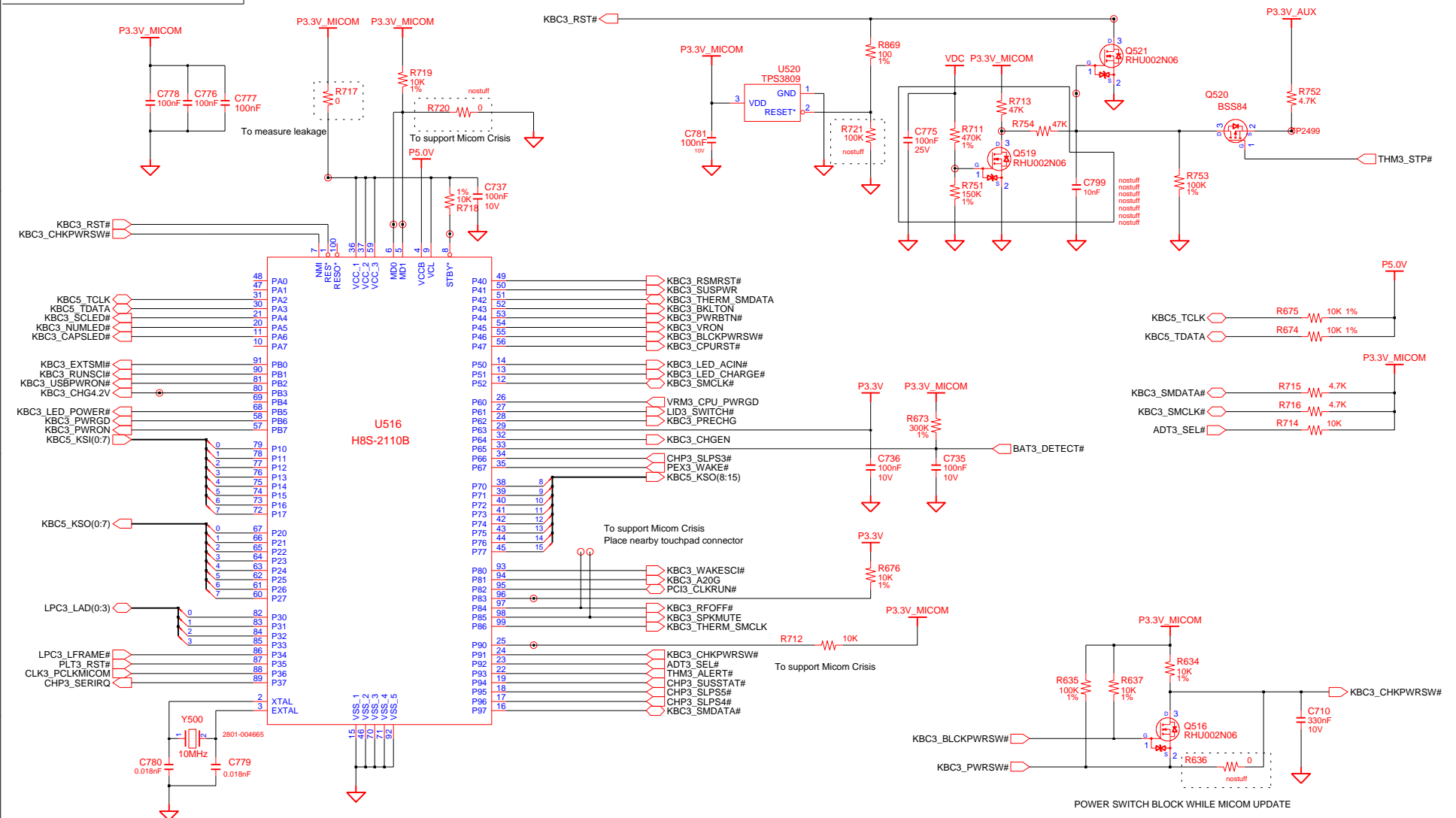
HEADPHONE



The traces led to Audio Jacks have the width over 10mil

DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	HDA_Codec_Alc262		
APPROVAL	SJ PARK	REV	1.0	HDA_Codec_Alc262 #4		
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM			
						PART NO. BA41-00920A
						PAGE 31 OF 64

MICOM RESET



MICOM Crisis Update

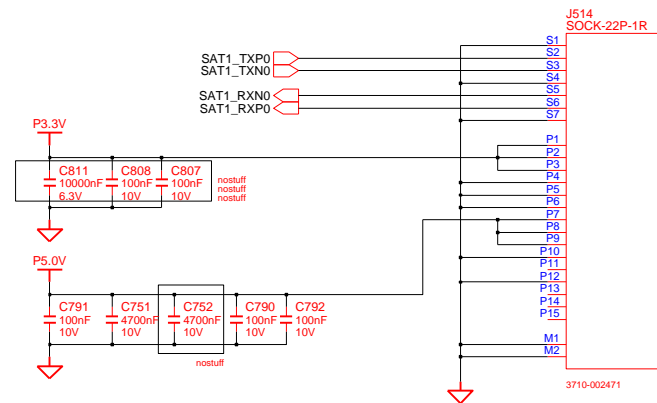
Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

DRAM	TERM1	DATE	1/10/2008	TITLE	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MICOM_Renesas2110_100p	
APPROVAL	SJ PARK	REV	1.0	MICOM_Renesas2110_100p	
MODULE CODE	LAST EDIT			PART NO. BA41-00920A June 09, 2008 11:54:01 AM	
				PAGE	47 OF 64

4

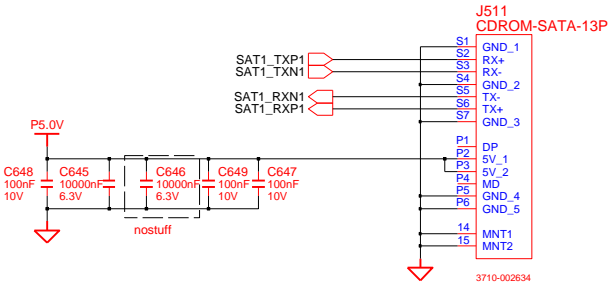
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Main to HDD



DRAW	TERMI	DATE	1/10/2008	TITLE LYON_External HDD_IF_Conn HDD_IF_Conn		SAMSUNG ELECTRONICS	
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0			PART NO.	BA41-00920A
MODULE CODE	LAST EDIT			June 09, 2008 11:54:01 AM	PAGE	33	OF 64

SATA ODD

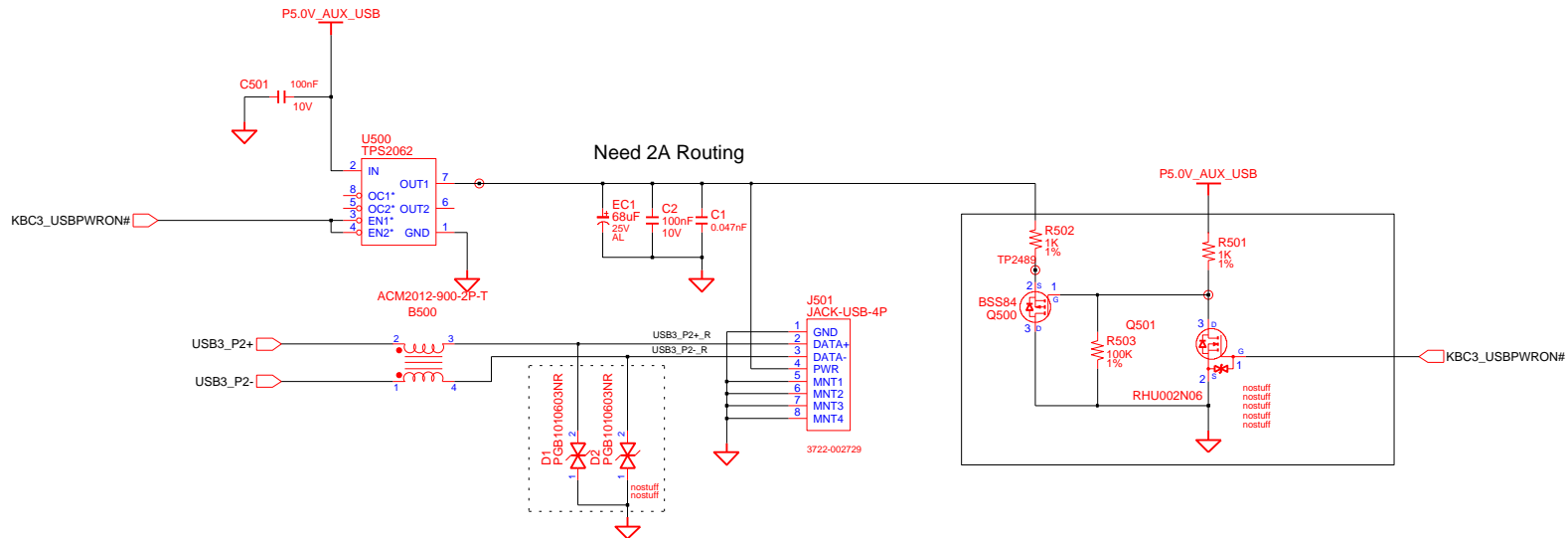


DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	ODD_IF_Conn		ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	ODD_IF_Conn	PART NO.	BA41-00920A
MODULE CODE	LAST EDIT			June 09, 2008 11:54:01 AM	PAGE	49 OF 64

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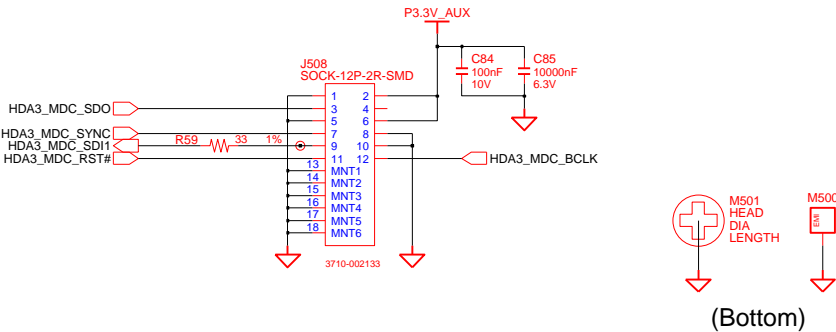
1 PORT USB CONNECTOR



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00920A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	63	OF 64

DRAM	TERMI	DATE	1/10/2008	TITLE	LYON_External USB_2Port USB_2Port	SAMSUNG ELECTRONICS		
CHECK	HJ KIM	DEV. STEP	MP					
APPROVAL	SJ PARK	REV	1.0				PART NO.	BA41-00920A
MODULE CODE	LAST EDIT		June 09, 2008 11:54:01 AM				PAGE 64 OF 64	

MDC Connector

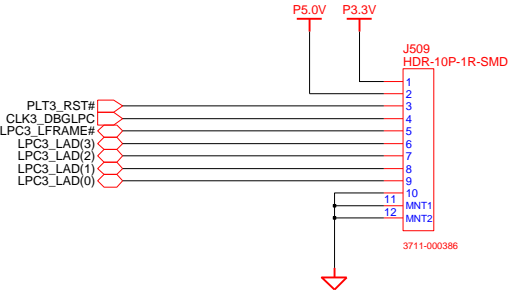


(Bottom)

DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	HDA_Modem	HDA_Modem	ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	HDA_Modem	HDA_Modem	PART NO. BA41-00920A
MODULE CODE	LAST EDIT June 09, 2008 11:54:01 AM				PAGE 32	OF 64

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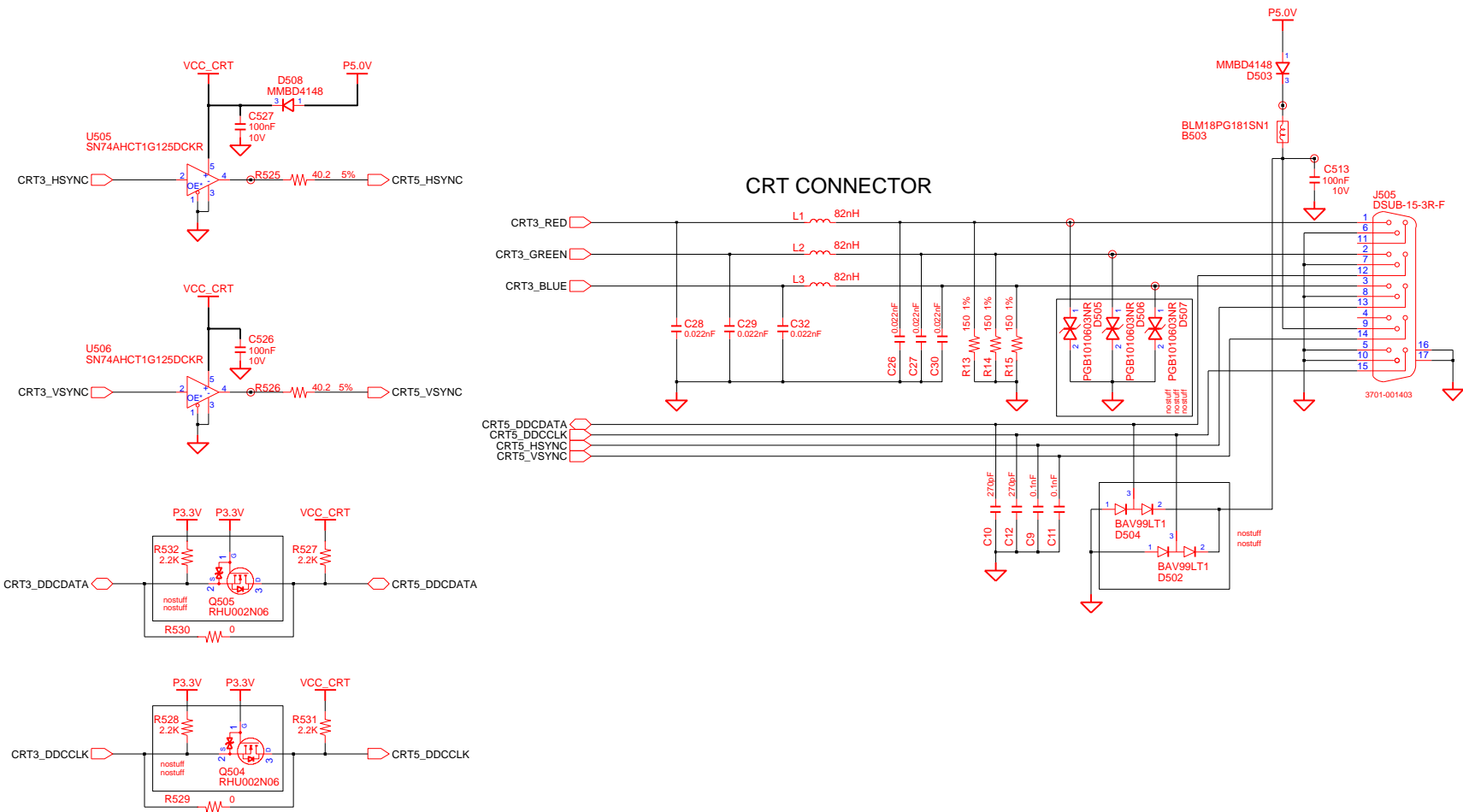
80H DECODER CONNECTOR



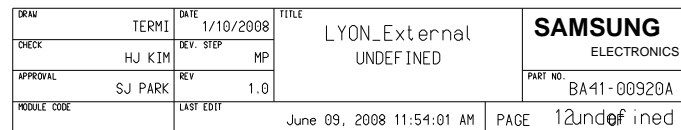
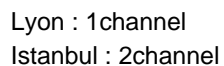
DRAW	TERMI	DATE	1/10/2008	TITLE		SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	Other_Debug_80		
APPROVAL	SJ PARK	REV	1.0	Other_Debug_80		
				PART NO. BA41-00920A		
MODULE CODE		LAST EDIT		June 09, 2008 11:54:01 AM		PAGE 50 OF 64

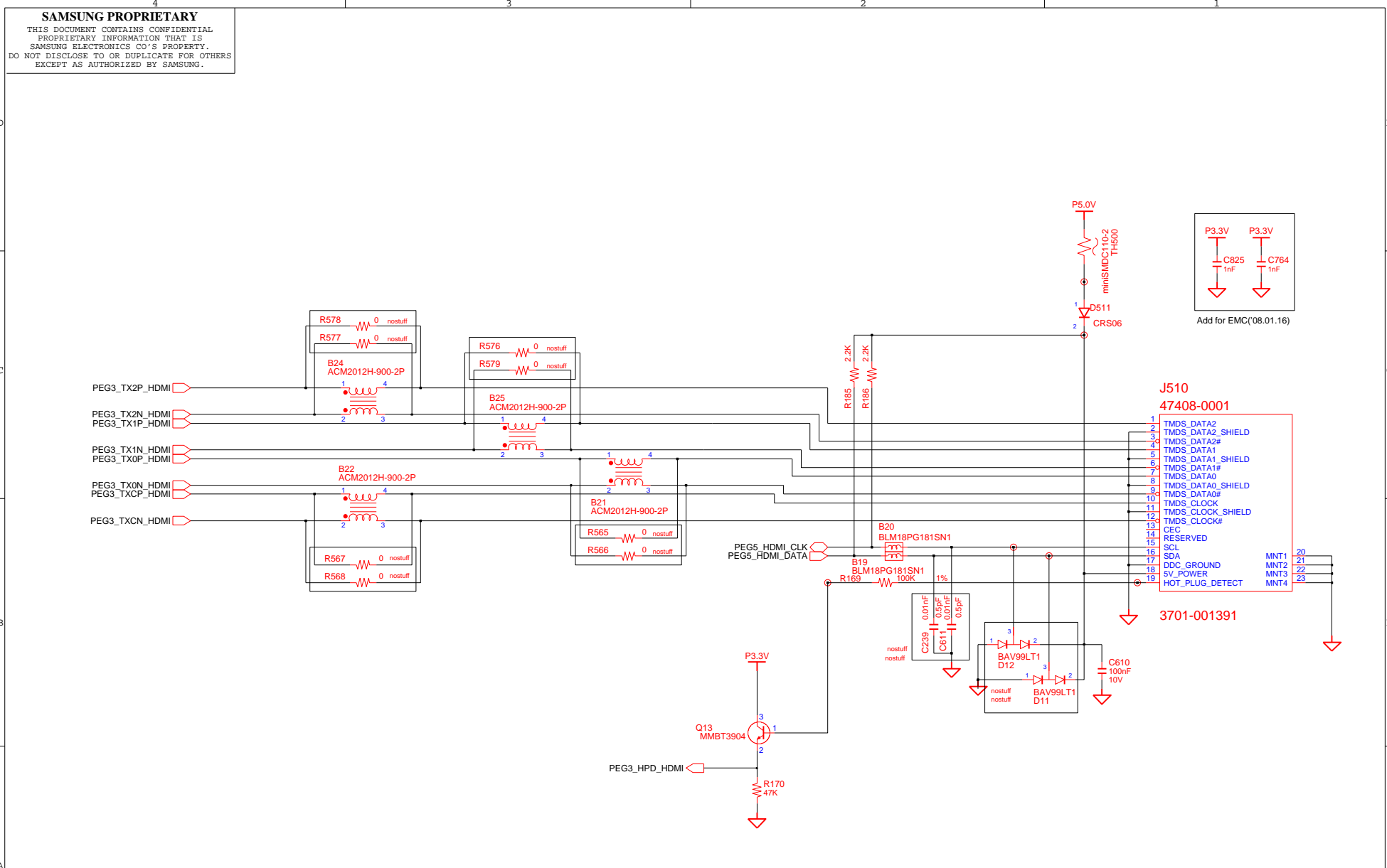
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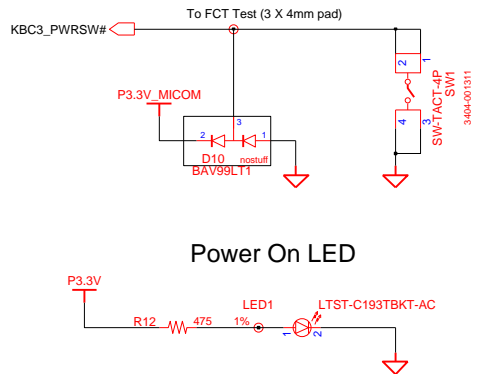


DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00920A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	25	OF 64





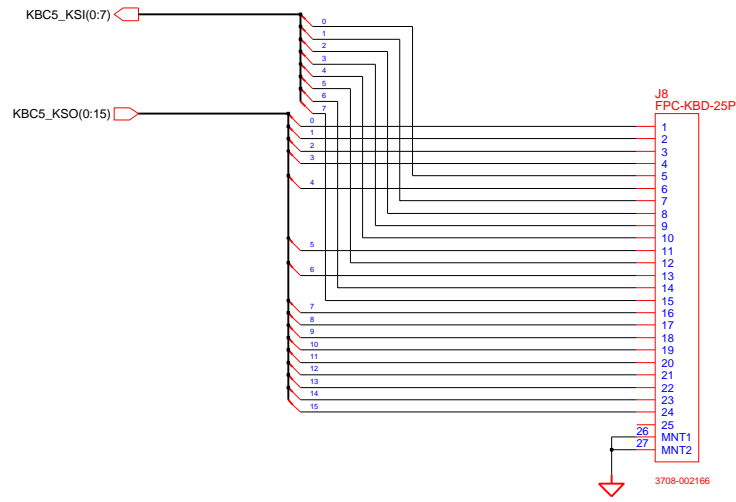
Put this LED located near PWRSW from ME recommendation
Power LED, Blue color



Power On LED

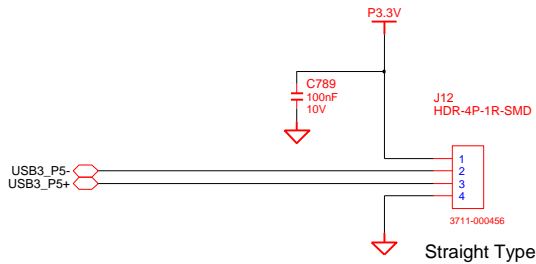
DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External MIO_Switch MIO_Switch	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	LAST EDIT			June 09, 2008 11:54:01 AM	PAGE	48 OF 64

KEYBOARD



DRAW	TERMI	DATE	1/10/2008	TITLE LYON_External KBD_IF_Conn KBD_IF_Conn		SAMSUNG ELECTRONICS		
CHECK	HJ KIM	DEV. STEP	MP					
APPROVAL	SJ PARK	REV	1.0					PART NO.
MODULE CODE		LAST EDIT		June 09, 2008 11:54:01 AM	PAGE	39	OF	64

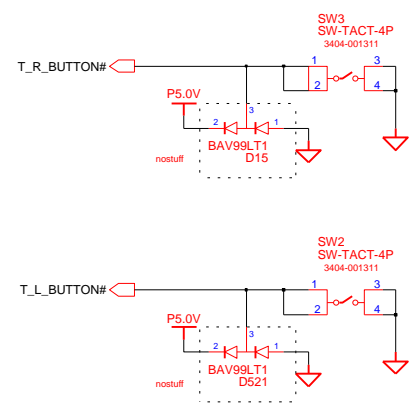
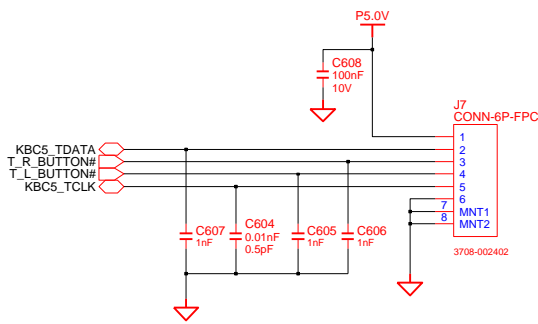
Bluetooth Interface



DRAW	TERMI	DATE	1/10/2008	LYON_External Bluetooth_IF_Conn Bluetooth_IF_Conn		SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT		June 09, 2008 11:54:01 AM		PART NO. BA41-00920A
				PAGE	19	OF 64

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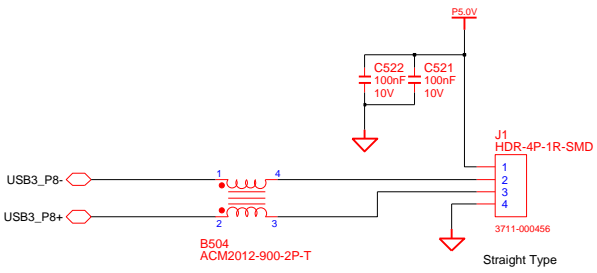
TOUCHPAD



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External Touchpad_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	62 OF 64	

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CAMERA



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	Camera_IF_Conn		
APPROVAL	SJ PARK	REV	1.0	Camera_IF_Conn	PART NO.	
MODULE CODE	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	20	OF 64	

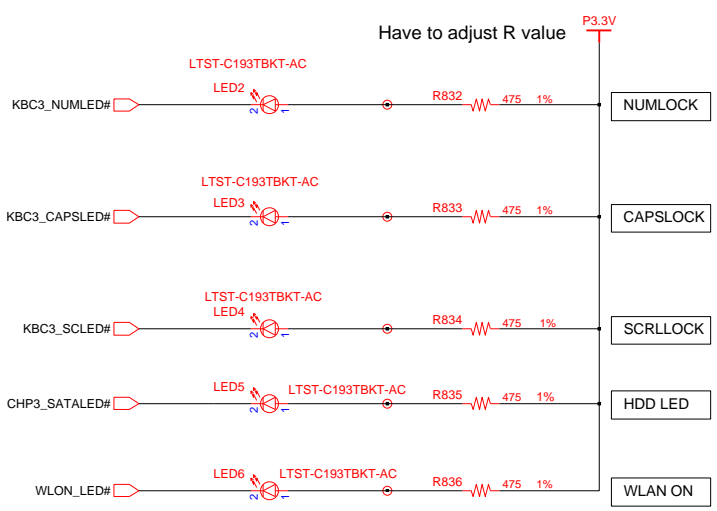
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D

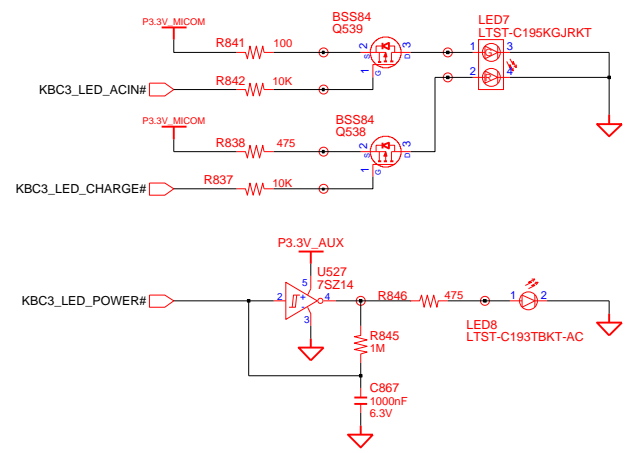
C

B

A



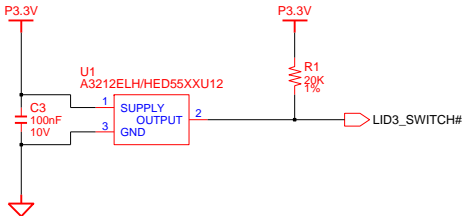
ADAPTERIN/CHARGING LED



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00920A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	40	OF 64

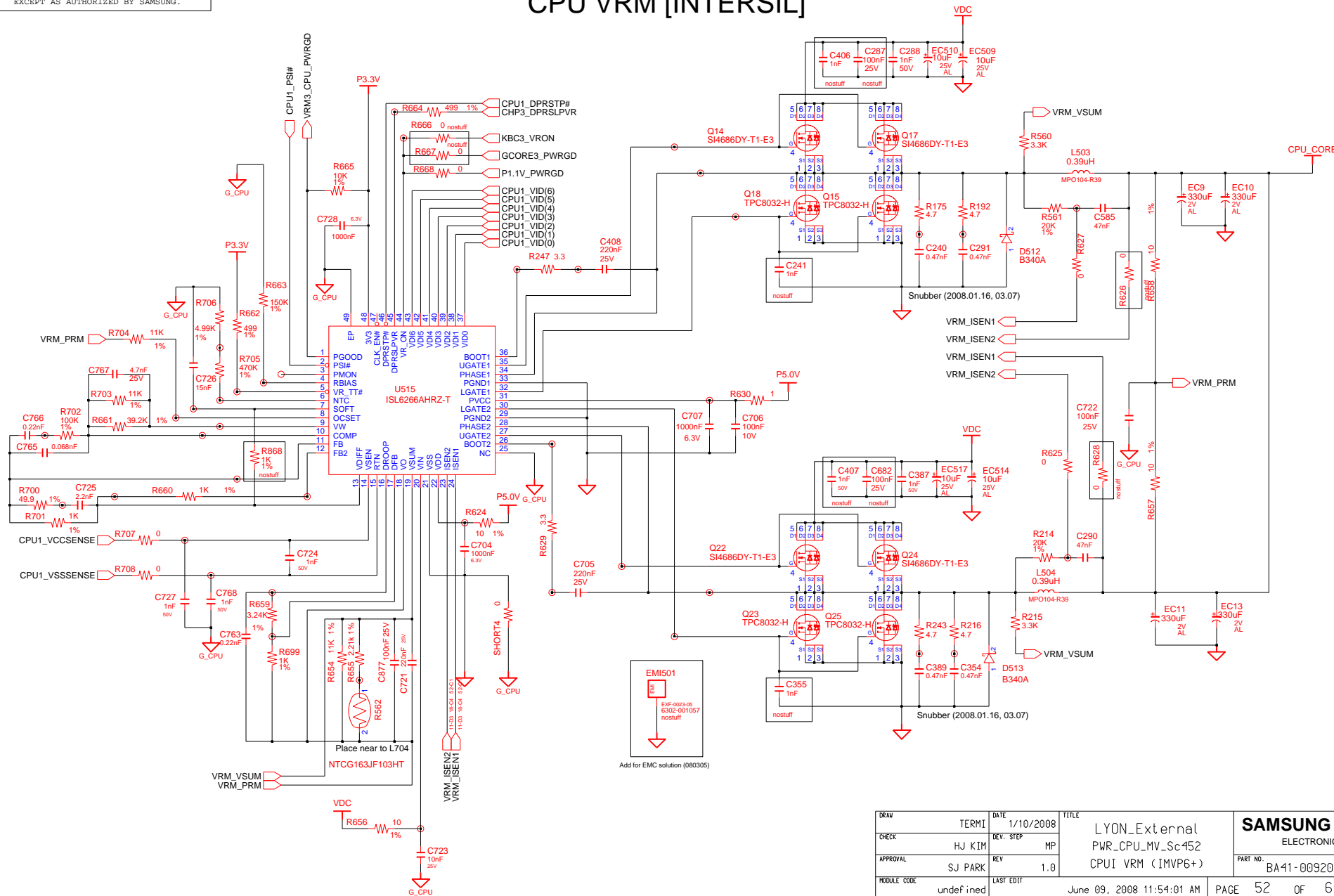
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LID_SWITCH



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External LID_Switch LID_Switch	PART NO.	SAMSUNG ELECTRONICS BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0				
MODULE CODE		LAST EDIT		June 09, 2008 11:54:01 AM		PAGE	41 OF 64

CPU VRM [INTERSIL]



DRAW		DATE	1/10/2008		TITLE		SAMSUNG ELECTRONICS	
TERMI		DEV. STEP	MP					
CHECK		HJ KIM		MP	LYON_External PWR_CPU_MW_Sc452 CPU1 VRM (IMVP6+)		PART NO.	
APPROVAL		SJ PARK		1.0			BA41-00920A	
MODULE CODE		undefined		LAST EDIT		June 09, 2008 11:54:01 AM		PAGE 52 OF 64

The schematic diagram illustrates the power management section of the BLM18SG260TN1, centered around the U512 SC4624MLTRT IC. The IC is configured with the following pin connections:

- VCC_1** (Pin 5) connected to P1.1V_PWRGD.
- PGOOD** (Pin 6) connected to P3.3V.
- AGND** (Pin 13) connected to G_P1.1V.
- SYNC_EN** (Pin 14) connected to G_P1.1V.
- NC_1** (Pin 7) connected to G_P1.1V.
- COMP** (Pin 10) connected to G_P1.1V.
- NC_3** (Pin 11) connected to G_P1.1V.
- FB** (Pin 12) connected to G_P1.1V.
- PH1** (Pin 18) connected to G_P1.1V.
- PH2** (Pin 19) connected to G_P1.1V.
- PH3** (Pin 20) connected to G_P1.1V.
- NC_2** (Pin 8) connected to G_P1.1V.
- PGND1** (Pin 15) connected to G_P1.1V.
- PGND2** (Pin 16) connected to G_P1.1V.
- THERM** (Pin 21) connected to G_P1.1V.

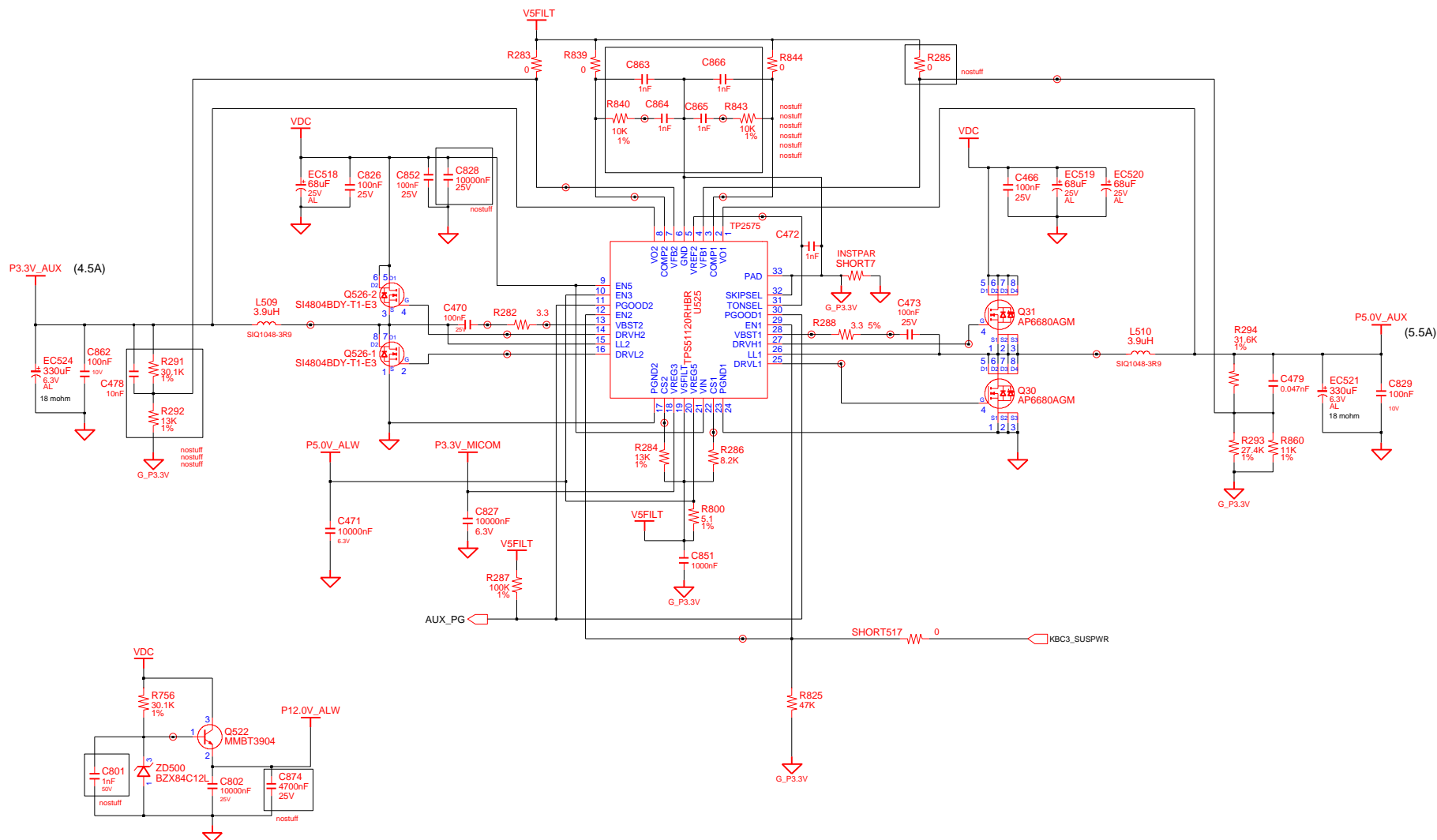
The IC is surrounded by various passive components:

- Capacitors:** C348 (1000nF, 6.3V), C383 (0.068nF), C384 (0.47nF, 50V), C379 (220uF, 2.5V AD), C381 (1nF, 50V), C382 (1nF, 50V), C380 (22000nF, 20%), C373 (22000nF, 20%).
- Resistors:** R236 (1K, 1%), R237 (1K, 1%, nostuff), R233 (27.4K, 1%), R232 (1K, 1%), R235 (22K, 1%), R207 (10), R206 (51.1K, 1%), C347 (22nF, 80V), C346 (47nF, nostuff), R205 (27.4k, 1%), L505 (2.2uH, SIQ1048-2R2), R596 (0, nostuff).

The diagram also shows the connection of the P1.1V (1.1075V) rail to the P1.1V_PWRGD and P1.1V inputs, and the P5.0V_AUX rail to the P5.0V_AUX input. The G_P1.1V ground rail is connected to the AGND, PGND1, and PGND2 pins of the IC.

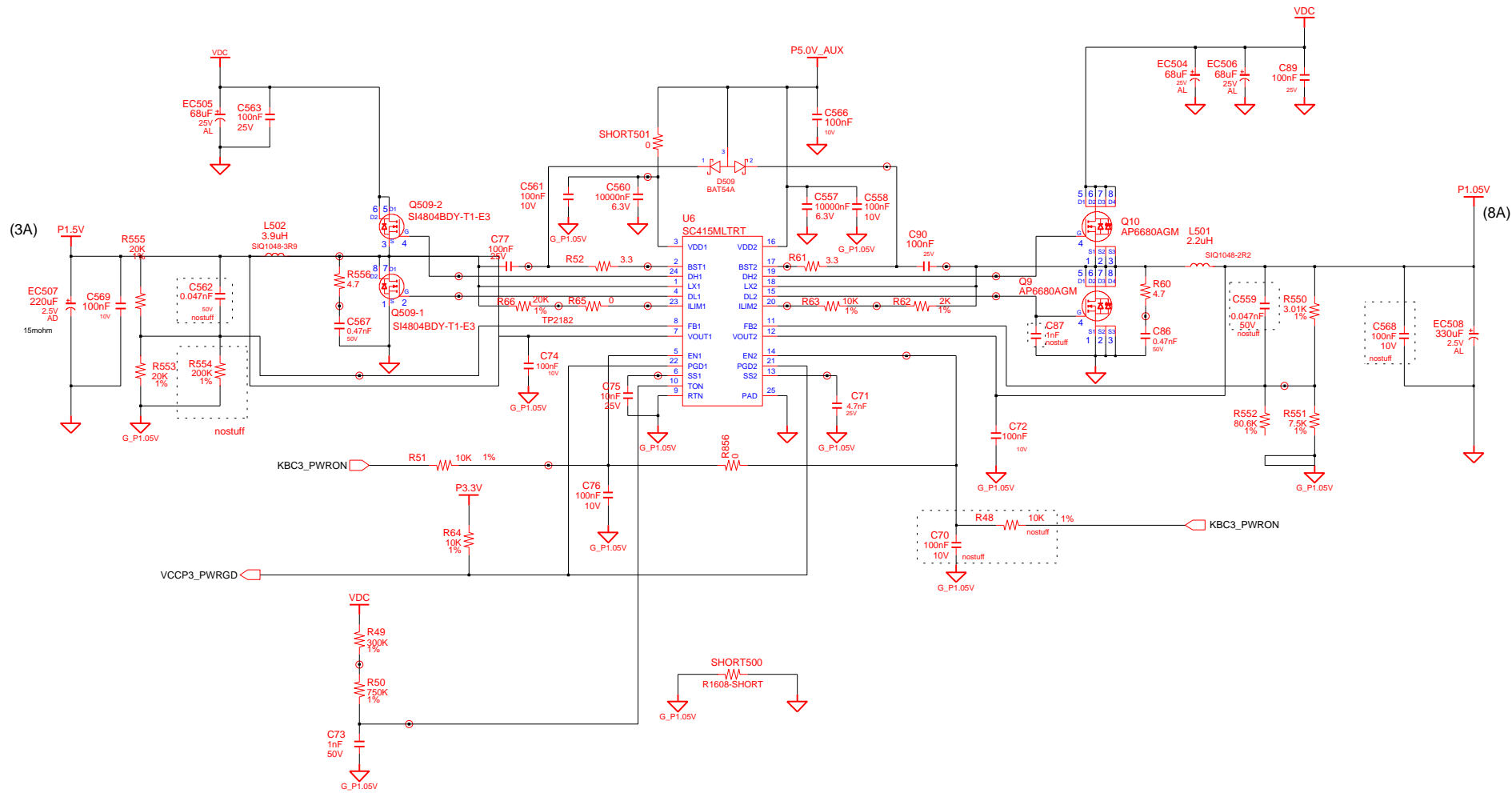
COM-22C-015(1996.6.5) REV. 3

P3.3V_AUX & P5.0V_AUX

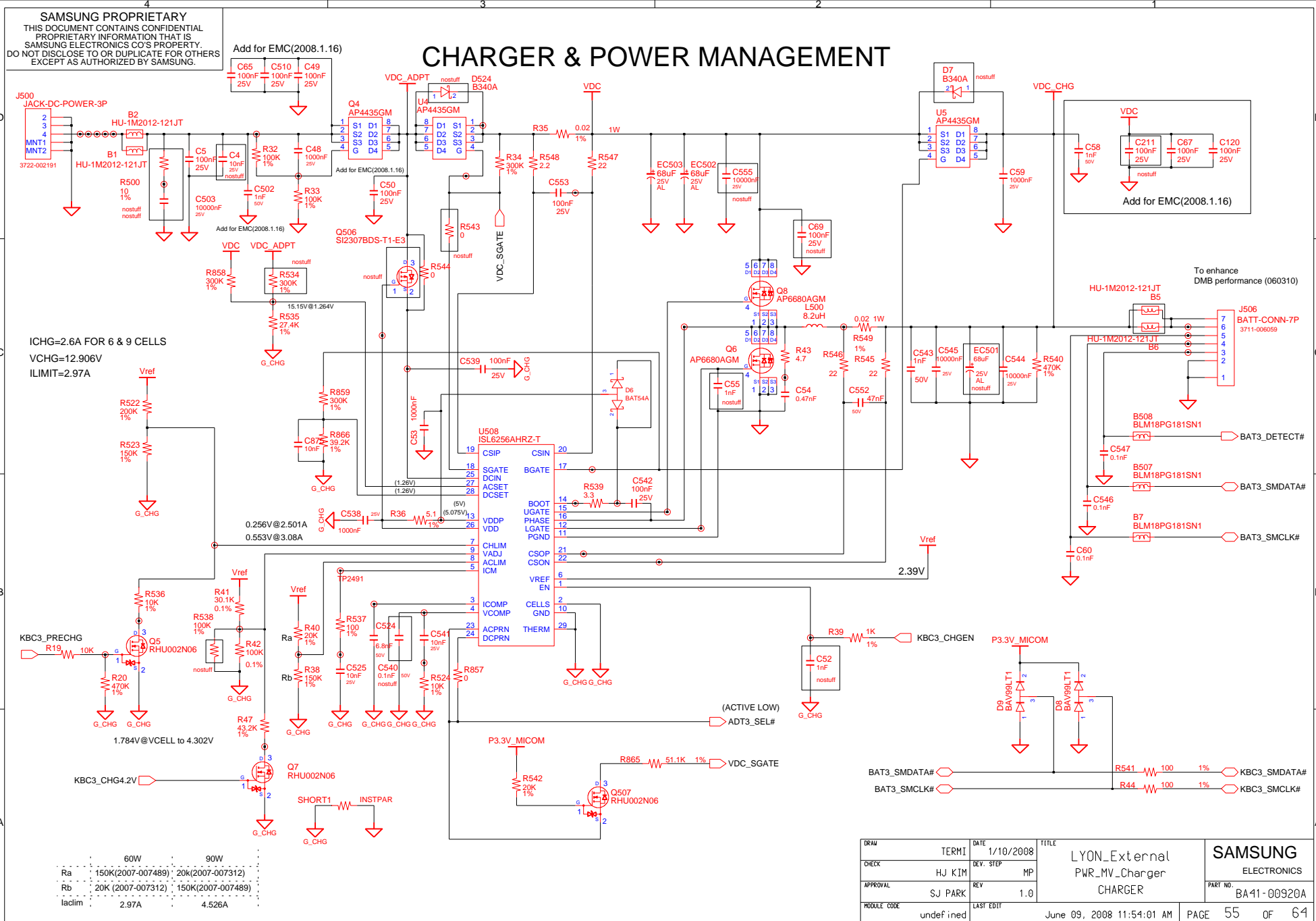


DATE	1/10/2008	TITLE	LYON_External PWR_MV_3V_5v P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
TERMI				
CHECK	HJ_KIM			
DESIGN	MP			
APPROVAL	REV	1.0	PART NO.	BA41-00920A
SJ_PARK				
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE 53 OF 64

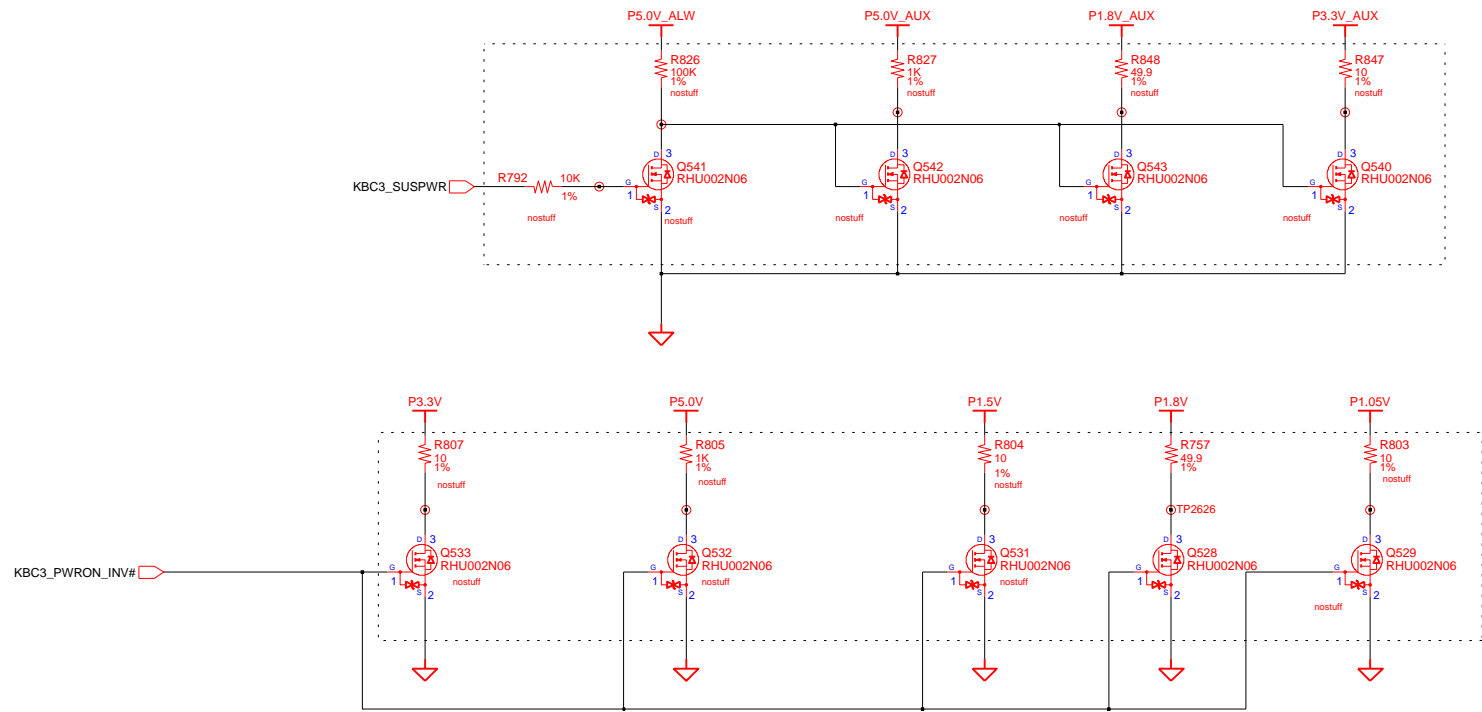
CHIPSET POWER (P1.05V & P1.5V)



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	PWR_MV_Cantiga	PWR_MV_Cantiga	ELECTRONICS
APPROVAL	SJ PARK	REV	1.0	Chipset Power (P1.05V-M, P1.2V)	PART NO.	BA41-00920A
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	54	OF 64



POWER DISCHARGER

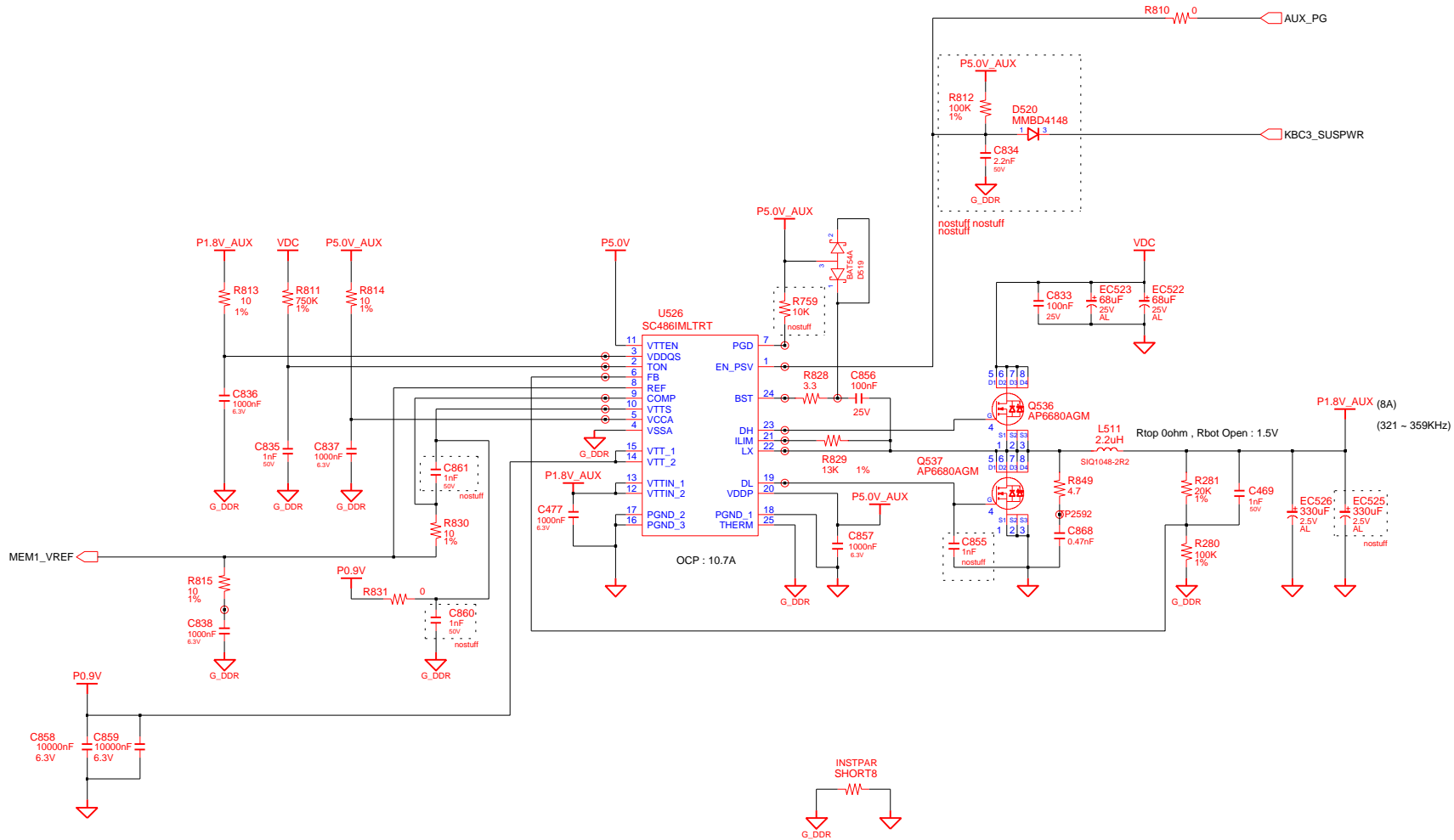


DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External PWR_MV_DisCharger DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			PART NO. BA41-00920A
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	56	OF 64

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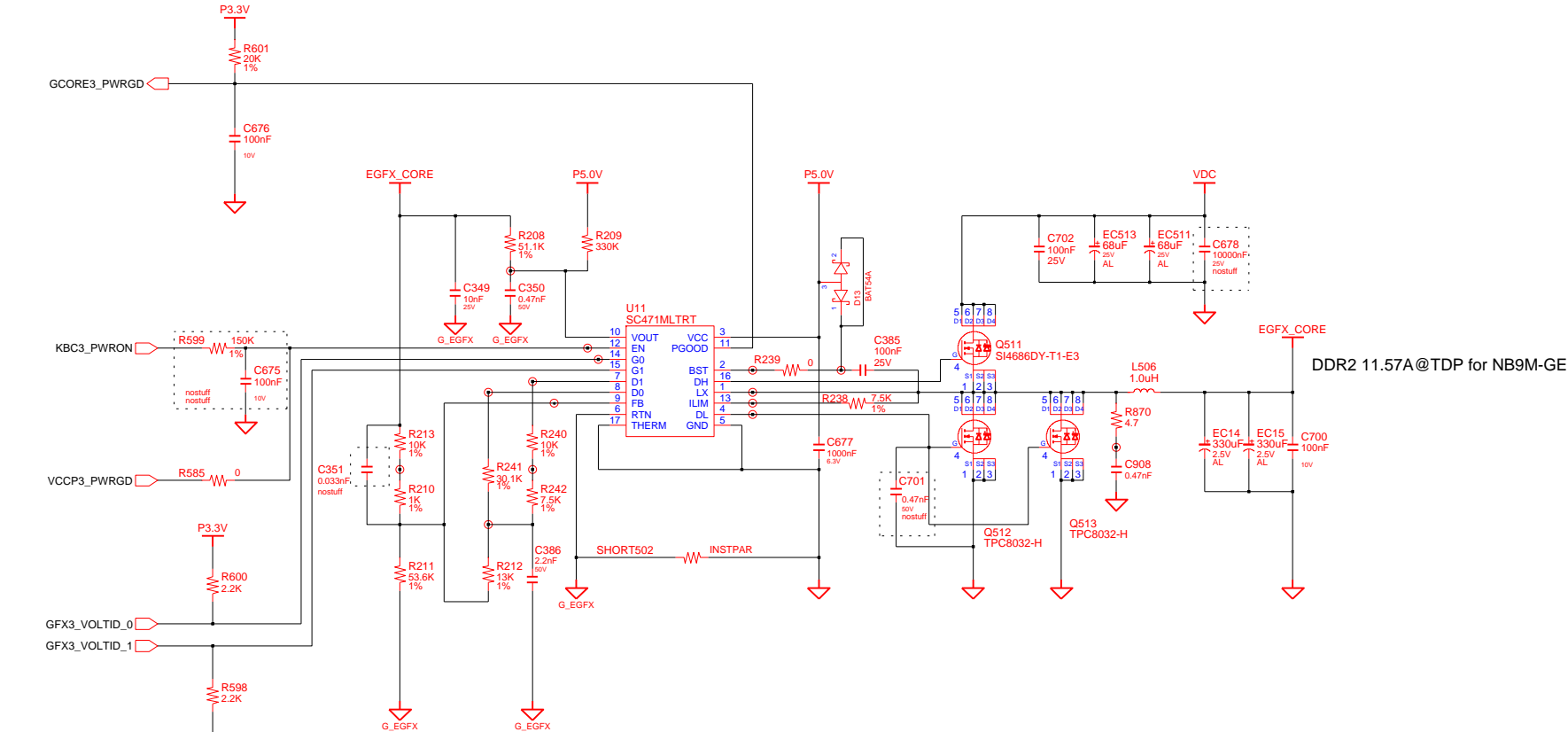
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DDR2 Power



DRAW	TERMI	DATE	1/10/2008	TITLE	LYON_External PWR_MV_MeMory	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	June 09, 2008 11:54:01 AM			
						PART NO. BA41-00920A
						PAGE 57 OF 64

Graphic Core Power



GFX3_VOLTID		
G0	G1	
0	0	0.9V (0.9??V)
1	0	1.09V (1.093V)
0	1	1.17V (1.175V)
1	1	RESERVE

DRAW	TERMI	DATE	8/14/2007	TITLE	LYON_External	SAMSUNG
CHECK	HJ KIM	DEV. STEP	MP	PWR_Gfx_MV_Ext	Elect Gfx Core(SC471)	ELECTRONICS
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00920A
MODULE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	2	OF 2

Sheet1 ----- Root[sheet1]
Sheet2 ----- Root[sheet2]
Sheet3 ----- Root[sheet3]
Sheet4 ----- Root[sheet4]
Sheet5 ----- Root[sheet5]
Sheet6 ----- Root[sheet6]
Sheet7 ----- Root[sheet7]
Sheet8 ----- Root[sheet8]
Sheet9 ----- Root[sheet9]
Sheet10 ----- Root[sheet10]
Sheet11 ----- Root[sheet11]
Sheet12 ----- Root[sheet12]
Sheet13 ----- Root[sheet13]
Sheet14 ----- Root[sheet14]
Sheet15 ----- Root[sheet15]
Sheet16 ----- Root[sheet16]
Sheet17 ----- Root[sheet17]
Sheet18 ----- Root[sheet18]
Sheet19 ----- Root[sheet19]
Sheet20 ----- CK_Clock_505M[sheet1]
Sheet21 ----- Thermal_Sensor_SMSC_Emc2102[sheet1]
Sheet22 ----- CPU_Penryn_MV_SV[sheet1]
Sheet23 ----- CPU_Penryn_MV_SV[sheet2]
Sheet24 ----- CPU_Penryn_MV_SV[sheet3]
Sheet25 ----- MCH_CANTIGA_GM_DDR2[sheet1]
Sheet26 ----- MCH_CANTIGA_GM_DDR2[sheet2]
Sheet27 ----- MCH_CANTIGA_GM_DDR2[sheet3]
Sheet28 ----- MCH_CANTIGA_GM_DDR2[sheet4]
Sheet29 ----- MCH_CANTIGA_GM_DDR2[sheet5]
Sheet30 ----- SODIMM_DDR2[sheet1]
Sheet31 ----- SODIMM_DDR2[sheet2]
Sheet32 ----- ICH_9M_B[sheet1]
Sheet33 ----- ICH_9M_B[sheet2]
Sheet34 ----- ICH_9M_B[sheet3]
Sheet35 ----- ICH_9M_B[sheet4]
Sheet36 ----- ICH_9M_B[sheet5]
Sheet37 ----- SPI_BIOS_ROM[sheet1]
Sheet38 ----- Gfx_External_Nvidia_Nb9x_64bit[sheet1]
Sheet39 ----- Gfx_External_Nvidia_Nb9x_64bit[sheet2]
Sheet40 ----- Gfx_External_Nvidia_Nb9x_64bit[sheet3]
Sheet41 ----- Gfx_External_Nvidia_Nb9x_64bit[sheet4]
Sheet42 ----- Graphics_Memory_Nvidia[sheet1]
Sheet43 ----- Graphics_Memory_Nvidia[sheet2]
Sheet44 ----- PCIE_Minicard_Slot[sheet1]
Sheet45 ----- HDA_Codec_Alc262[sheet1]
Sheet46 ----- HDA_Codec_Alc262[sheet2]
Sheet47 ----- HDA_Codec_Alc262[sheet3]
Sheet48 ----- HDA_Codec_Alc262[sheet4]
Sheet49 ----- MICOM_Renesas2110_100p[sheet1]
Sheet50 ----- HDD_IF_Conn[sheet1]

Sheet51 ----- ODD_IF_Conn[sheet1]
Sheet52 ----- USB_1Port[sheet1]
Sheet53 ----- USB_2Port[sheet1]
Sheet54 ----- HDA_Modem[sheet1]
Sheet55 ----- Other_Debug_80[sheet1]
Sheet56 ----- Graphics_IF_CRT[sheet1]
Sheet57 ----- Graphics_IF_CRT[sheet2]
Sheet58 ----- Graphics_IF_CRT[sheet3]
Sheet59 ----- MIO_Switch[sheet1]
Sheet60 ----- KBD_IF_Conn[sheet1]
Sheet61 ----- Bluetooth_IF_Conn[sheet1]
Sheet62 ----- Touchpad_IF_Conn[sheet1]
Sheet63 ----- Camera_IF_Conn[sheet1]
Sheet64 ----- LED_Switch[sheet1]
Sheet65 ----- LID_Switch[sheet1]
Sheet66 ----- PWR_CPU_MV_ISL6262[sheet1]
Sheet67 ----- PWR_Gfx_MV_Ext[sheet1]
Sheet68 ----- PWR_MV_3V_5V[sheet1]
Sheet69 ----- PWR_MV_Cantiga[sheet1]
Sheet70 ----- PWR_MV_Charger_ISL6256[sheet1]
Sheet71 ----- PWR_MV_DisCharger[sheet1]
Sheet72 ----- PWR_MV_MeMory[sheet1]
Sheet73 ----- PWR_Gfx_MV_Ext[sheet2]